MASTER THE FUNDAMENTALS OF POWER INTEGRITY AND POWER SUPPLY TESTING

TESTING EXERCISES

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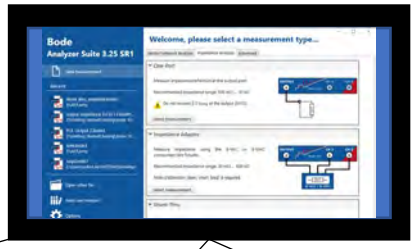
Test Equipment

Oscilloscope

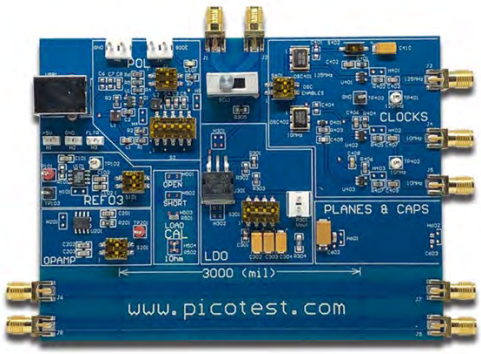
Bode Analyzer Suite



Bode 100

Keyboard

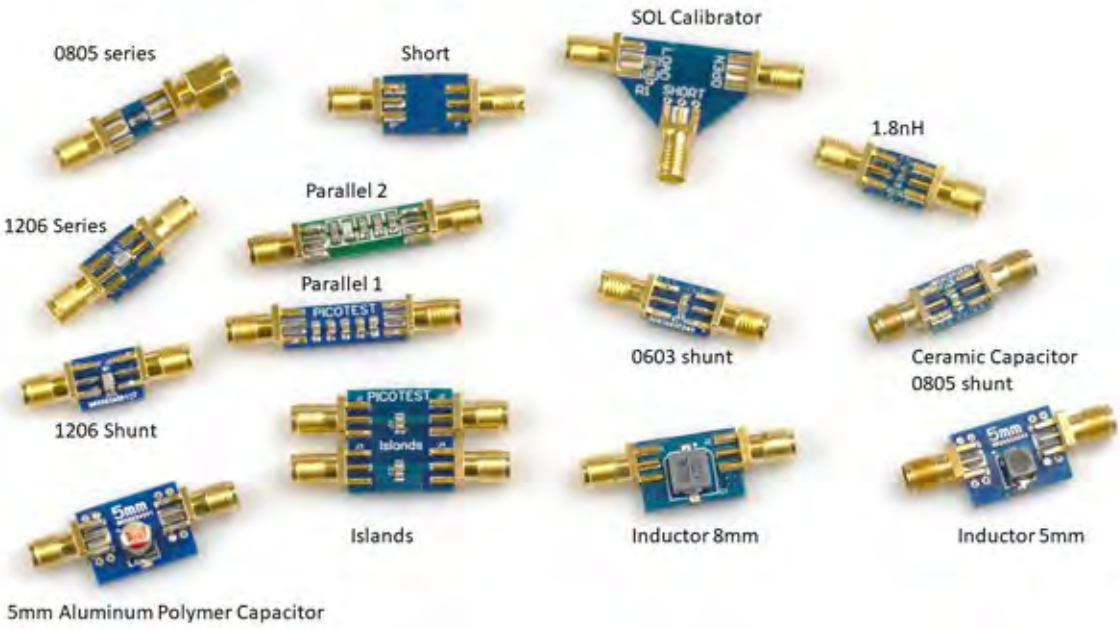
VRTS1P5



VRTS3

PITK01

LM20143B
Flat and Not Flat



Components in the Parts Kit (PITK01)

Signal Injectors

J2121A
High Power
Line Injector

J2102B
Common Mode Transformer*

J2120A
Line Injector

J2113
Differential Amplifier

J2111B
Current Injector

DC Blocker

P2130A

J2154A
PerfectPulse® Differential TDR

J2100A/J2101A/BWIT
Injection Transformer^

Measurement Accessory	PDN Probes	Current Injector	Preamplifier	DC Blocker	Common Mode Xfmr	GP Port Adapter	TDR	Injection Transformer	Line Injector	Current Probe
1-port Reflection 0.5Ω-2.5kΩ	X			X						
2-port Shunt Thru (GP) 25uΩ-25Ω	X		X	X		X				
2-port Shunt Thru Port 1-2 - 25uΩ-25Ω	X		X	X	X					
2-port Series Thru 25Ω-1MΩ	X									
3-port voltage/current 1mΩ-2kΩ	X	X	X		X					X
1-port TDR 10mΩ-1kΩ	X			X			X			
2-port TDT 10mΩ-1kΩ	X			X	X		X			
Bode Plot/Stability								X		
Non-Invasive Stability Measurement (NISM)	X	X		X						
PSRR		X	X		X				X	
Picotest Accessory	P2102A P2104A	J2111B J2112A	J2180A B-AMP12	J2130A P2130A	J2102B/ J2113A *Differences	J2160A (E5061B)	J2154A	J2100A J2101A BWIT ^Comparison	J2120A J2121A J2123A J2124A	Rogowski

https://www.picotest.com/products_injectors.html

Probes

[P2102A](#)
2-Port Probe

[P2106A](#)
Resistive Probe

[P2105A](#)
TDR Probe

[P2104A](#)
1-Port Probe

Measurement Accessory	2-Port Probe	1-Port Probe	TDR Probe	Resistive Probe	Differential TDR Probe
Impedance Measurement	X	X			
Low Impedance Measurement	X				
2-Port Impedance	X	X (Need 2)	X		
TDR	X	X	X		
Noise	X	X		X	
Step Load	X	X			
High Voltage				X	
NISM	X	X			
Ripple	X	X			
Clock Jitter	X	X			
Picotest Accessory	P2102A	P2104A	P2105A	P2106A	P2103A

Additional Resources:
https://www.picotest.com/images/download/Probe_Manual_1.53.pdf

Measurement Fundamentals

Introduction:
Noise is all around us. It is crucial that we know how our instruments like oscilloscopes, voltage network analyzers, frequency response analyzers, and even cables can affect our measurement. Your results are only as accurate and precise as your least precise and least accurate instrument. Therefore, we must understand the limitations of our instruments and what noise or artifacts they present in our measurement.

Oscilloscope Noise Floor: This shows the noise present in a measurement when using an oscilloscope. All oscilloscopes vary in the amount of noise present during the measurement. This can tell a person to what extent can I use this oscilloscope to make a measurement.

Impedance Matching: We need to match the impedance between the cable and the instrument. Otherwise, signal reflections can obstruct the measurement and cause very wrong measurements.

VNA Noise Floor: Similar idea to the oscilloscope noise floor experiment. We will be using the VNA for many measurements and must understand how the VNA will affect a measurement

Cable Matching: Matching the impedance with the cables will lead to a flat frequency response. We want to minimize resonances as resonances increase noise significantly. The length of the cable can be significant. Phase is related to length, but good calibration can alleviate that. A longer cable has more length for noise to enter but shield attenuation can help. A longer cable also has more shield resistance that can be corrected through a common mode isolator.

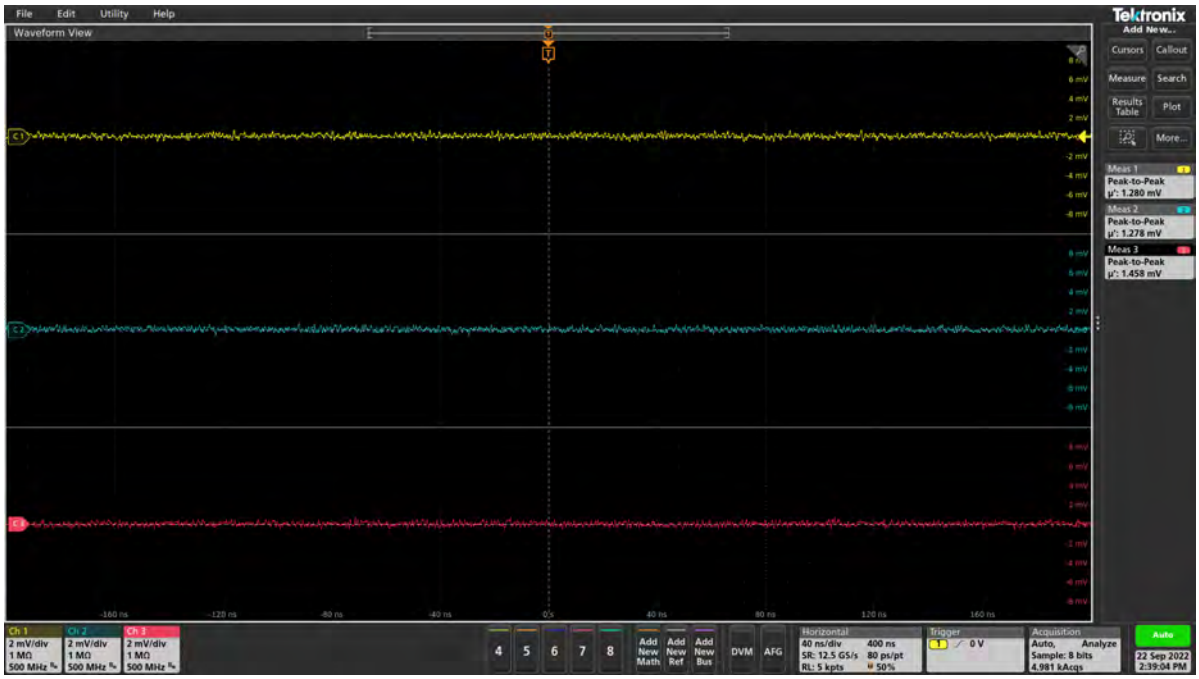
Oscilloscope Noise Floor

Description:
The noise floor is one of the most basic test limitations when performing a measurement. The limitations of the noise floor can be determined by looking at the RMS noise of the oscilloscope, which can be measured by using the measurement functions of the oscilloscope itself.

Instrument	Oscilloscope
Injectors	NA
Probe point	NA
Probes	NA

Setup File: Open the setup file **osc noise floor.tss**
Measurement Steps:
1. Turn on your oscilloscope.
2. Hit default setup.
3. Turn on Ch1, Ch2, and Ch3.
4. Set all channels to 1MΩ termination.
5. Measure the Voltage Peak to Peak (Vpp).

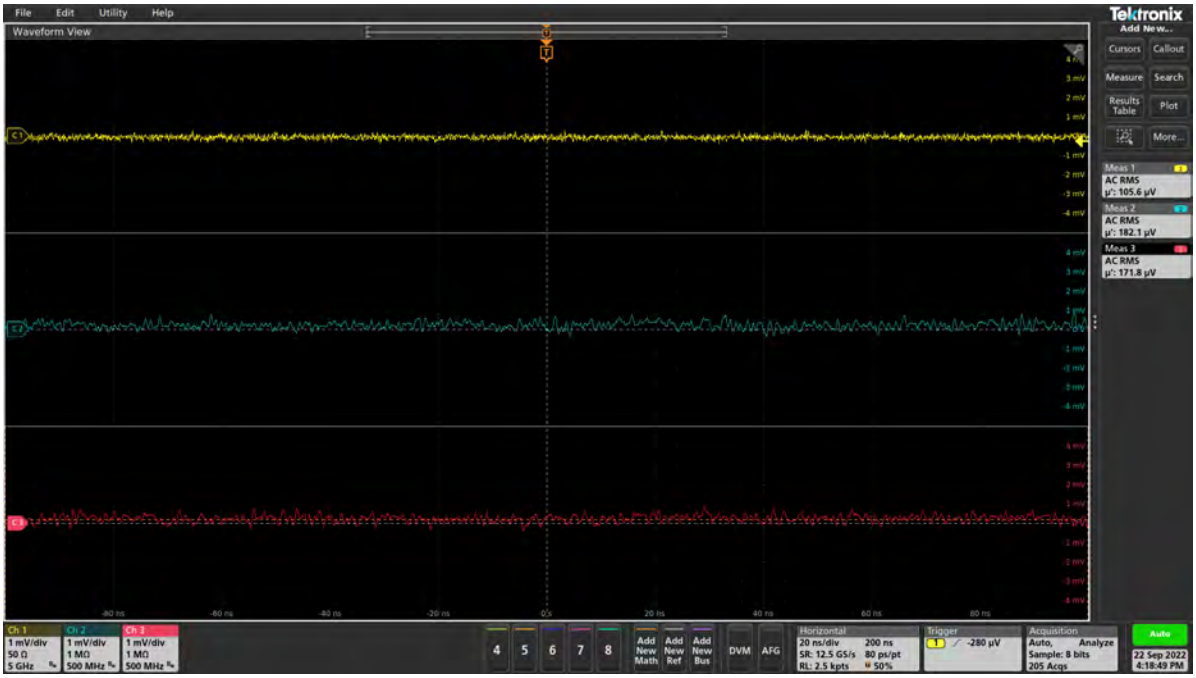
Results:



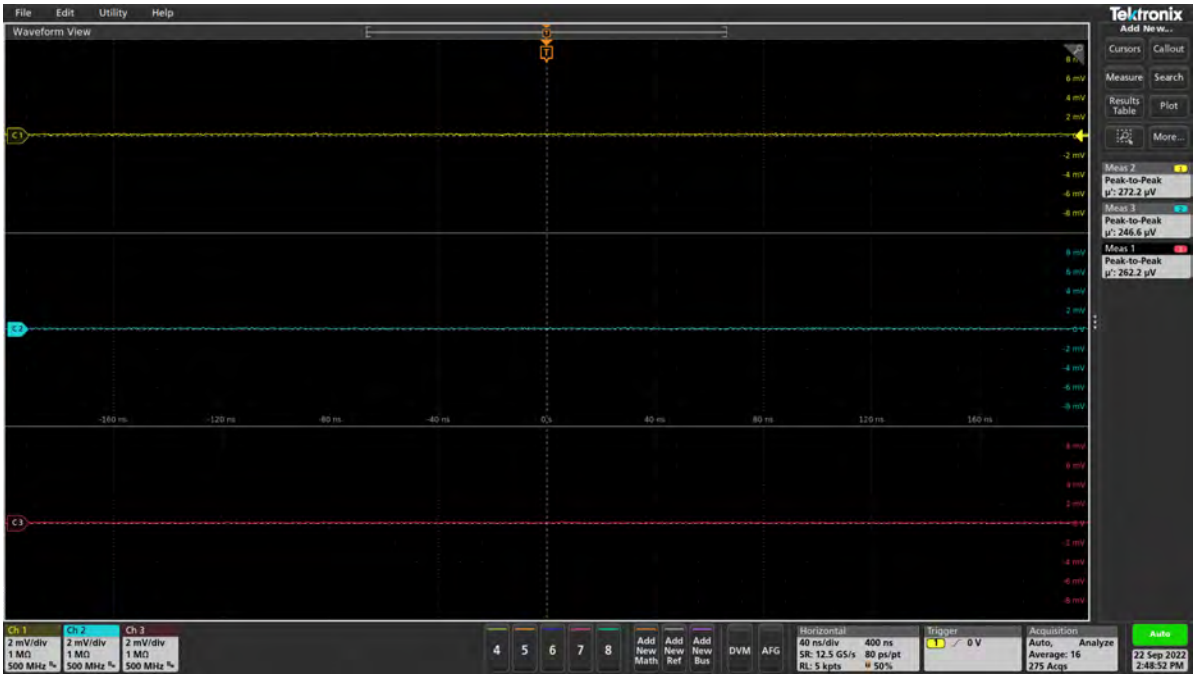
The Vpp for Ch1 is 1.28mV, Ch2 is 1.27mV, and Ch3 is 1.458mV.

Other things to try:

- Change the **measurement** from peak-to-peak voltage to AC root mean square (RMS).

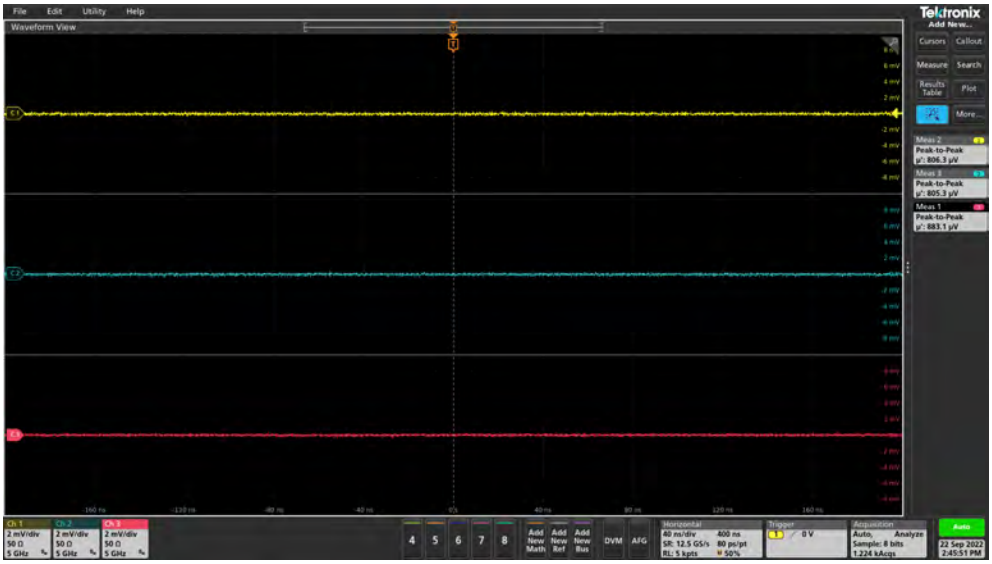


- Change the **acquisition** to averaging (this is in the bottom "Horizontal" window).



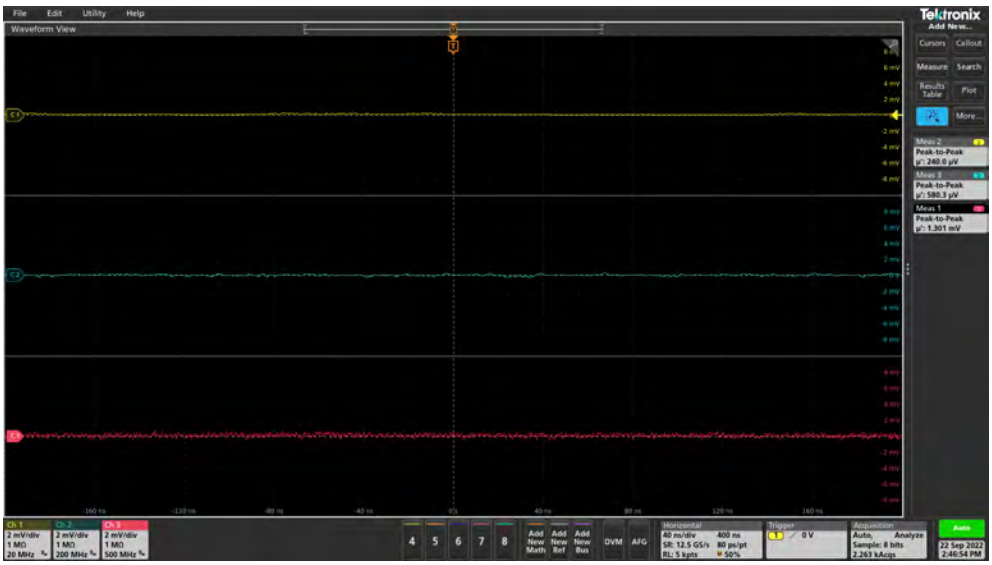
Other things to try:

- Change the **impedance** from 1MΩ to 50Ω.



Why is the noise higher when the impedance is changed even though the impedance is lower?

- Change the **bandwidth**. I set Ch1 to 20MHz and Ch2 to 200MHz. I left Ch3 at 500MHz.



Hopefully, we know how to look at the noise floor for our scopes. This allows us to know the capabilities of our scope. Remember, that not all channels are the same. Some will have less noise than others. Pick the correct device and channel that suit the measurement needs.

Additional Resources (Power Integrity Book, pages 22-30):

Impedance Matching

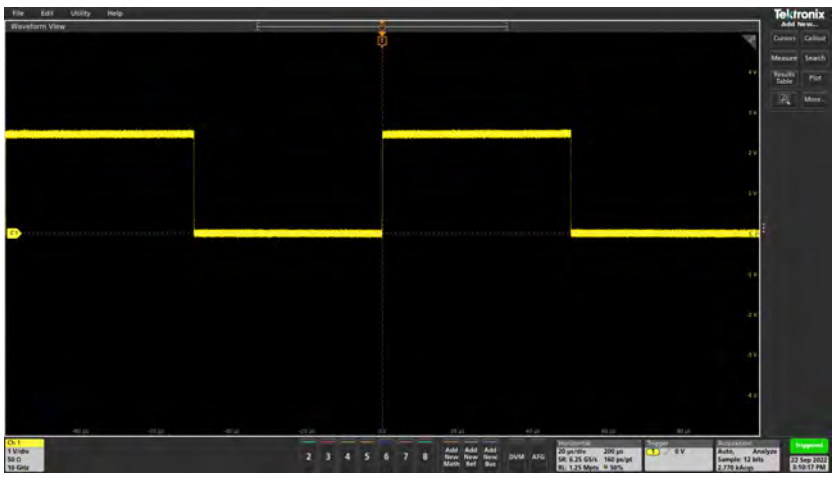
Description:
Proper impedance matching is required in order to make measurements correctly. At least one side of the measurement should match the impedance of the cable being used in the measurement. This test measures a signal and shows how the measurement can be affected by proper and improper impedance matching.

Instrument	Oscilloscope
Injectors	P2130A (Optional), 1Ω Resistor (Optional)
Probe point	N/A
Probes	N/A

Setup file: Open the setup file **imp match.tss**
Measurement Steps:
1. Turn on your oscilloscope.
2. Hit default setup.
3. Turn on Ch1
4. Set 50Ω termination.
5. Set the function generator so a 10kHz Pulse with a 2.5Vpp and a 1.25 DC Offset.
6. Connect the function generator to Ch1 of the oscilloscope.

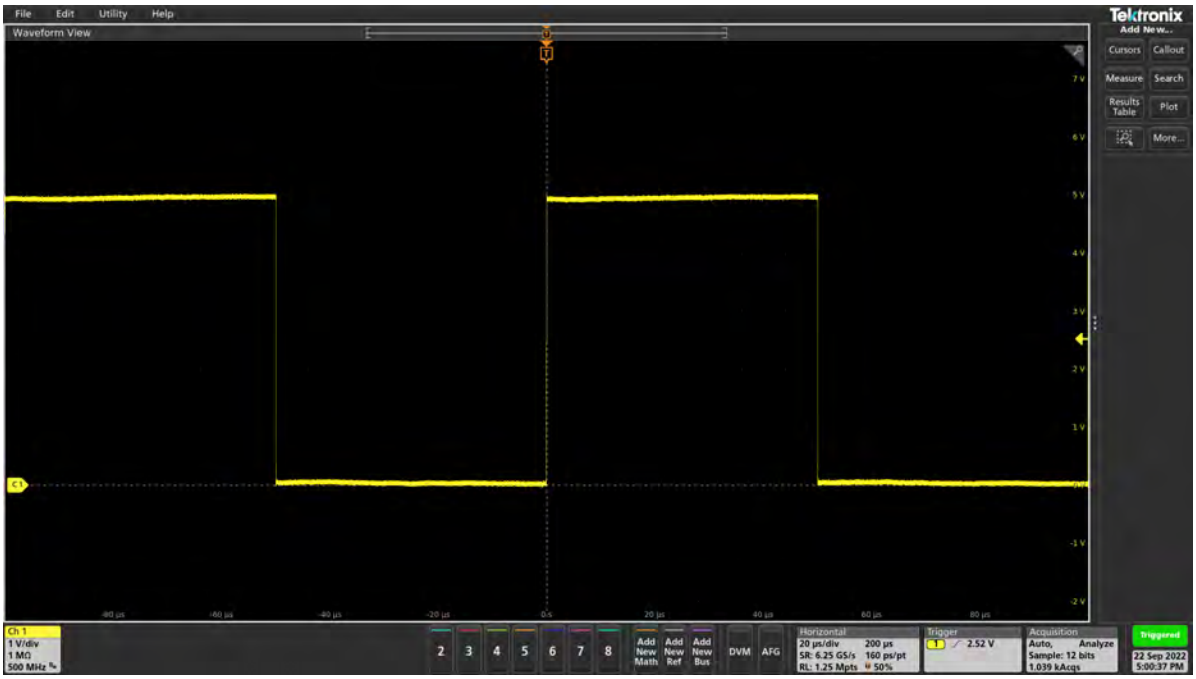
Setup Diagram:

Results:



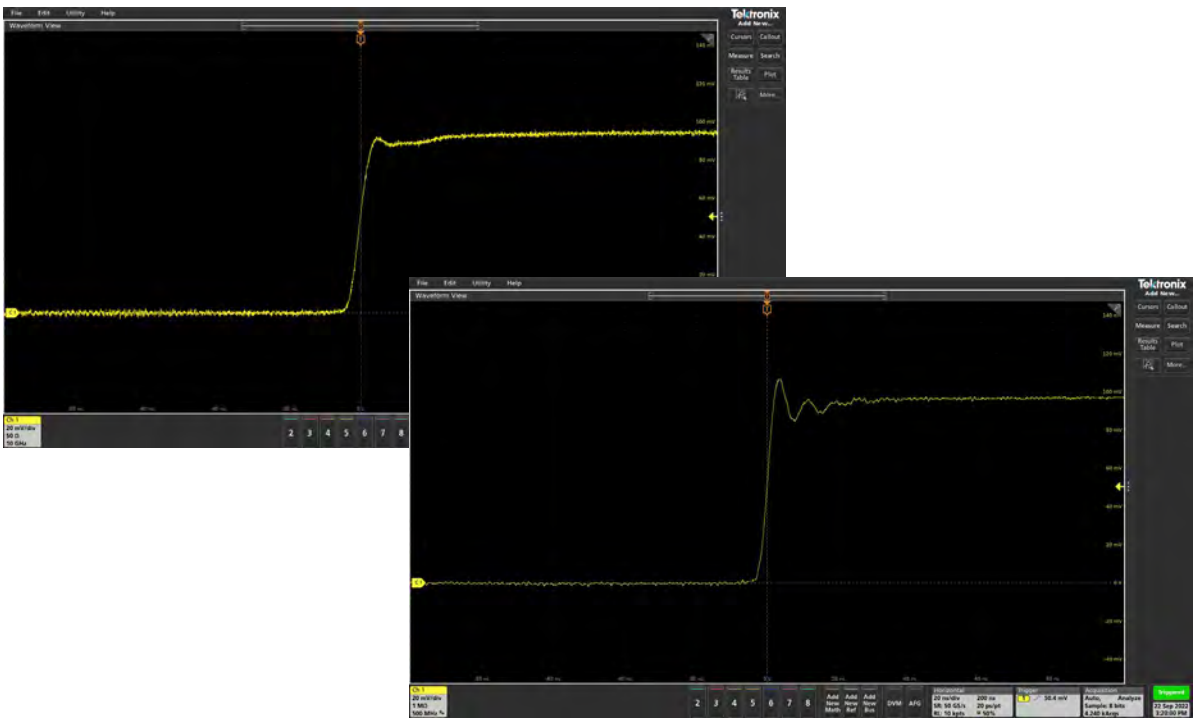
Other things to try:

- Change the termination to 1MΩ and observe the change in signal amplitude due to the mismatch.



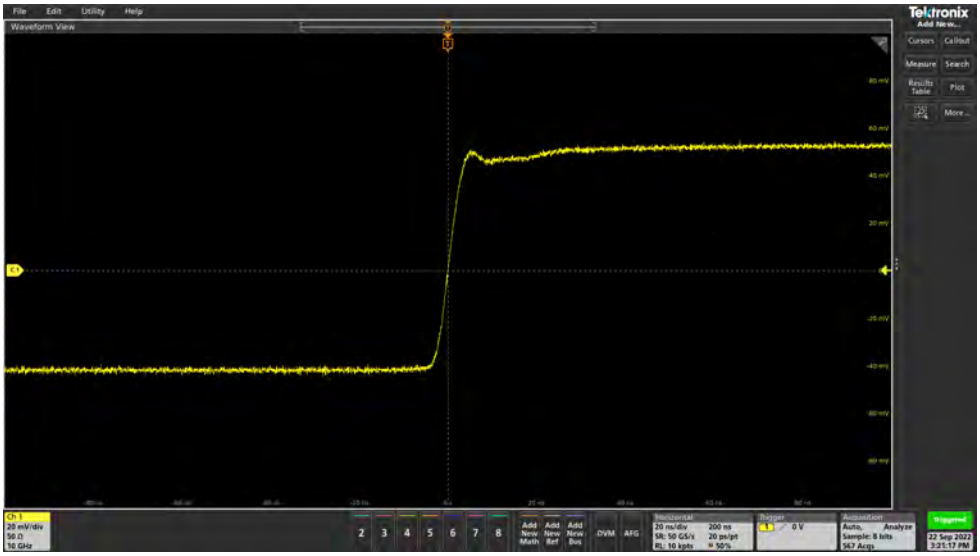
Other things to try:

- Repeat the measurement with a 1Ω shunt between the function generator and the oscilloscope. You will want to zoom into the leading edge to see the ringing due to mismatch. The left one is with 50Ω termination while the right is with 1MΩ.



Other things to try:

- Add a P2130A DC Blocker between the oscilloscope and the 1Ω shunt (Diagram below). Notice the change in DC offset.



Hopefully, you know how matching affects the measurement. With improper matching, we get wrong measurements. This can be used to determine the impedance of cables. If the cables have a good output impedance, then we know that it matches the impedance of the source.

Additional Resources:

http://www.edn.com/design/test-and-measurement/4433242/4/Match-impedances-when-making-measurements

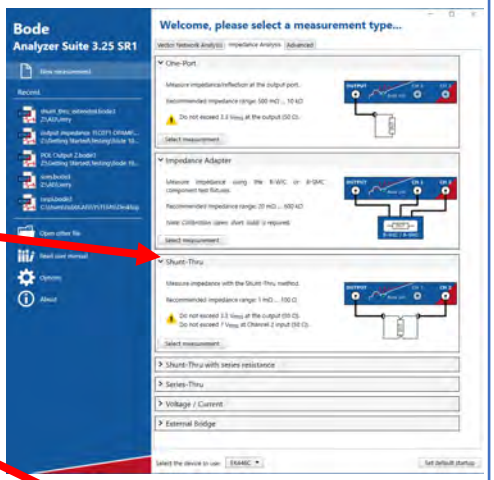
http://www.edn.com/design/test-and-measurement/4438691/2/Cable-tips-for-your-next-measurement

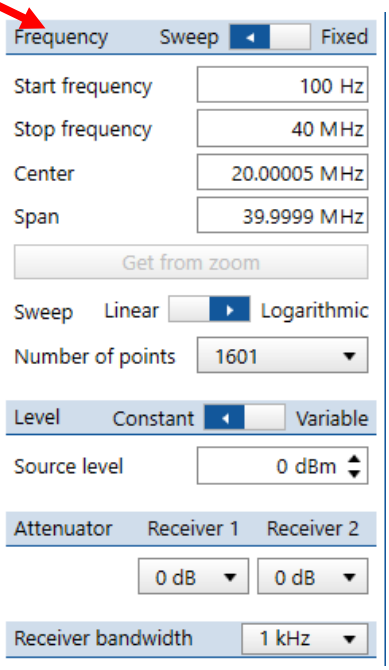
VNA Noise Floor

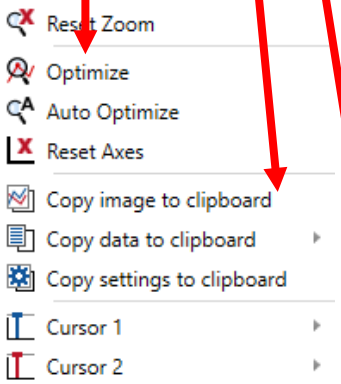
Description:
The measurement of low impedances can be difficult due to the limitations of various measurement techniques and test equipment. The two-port shunt-thru method allows the measurement of ultra-low impedance values (µohms to ohms) and is the predominant measurement for PDN applications.

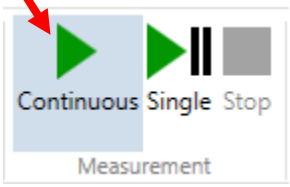
Testing the Noise Floor:

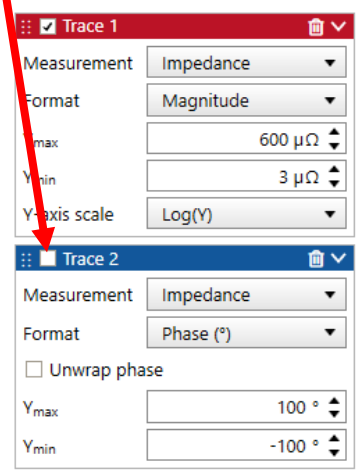
1. Start the Bode 100 software.
    - No connections are necessary for this test.
2. Select “Impedance Analysis”
3. Select “Shunt-Thru”
4. Set the parameters in the left panel to the values in the image below.
5. Start the Continuous sweep mode by clicking the “Continuous” button in the top right.
6. In the right panel uncheck the box for Trace 2.
7. Right-click the measurement window and select “Optimize”
8. You can export your measurements by right clicking on the measurement window selecting the appropriate option.



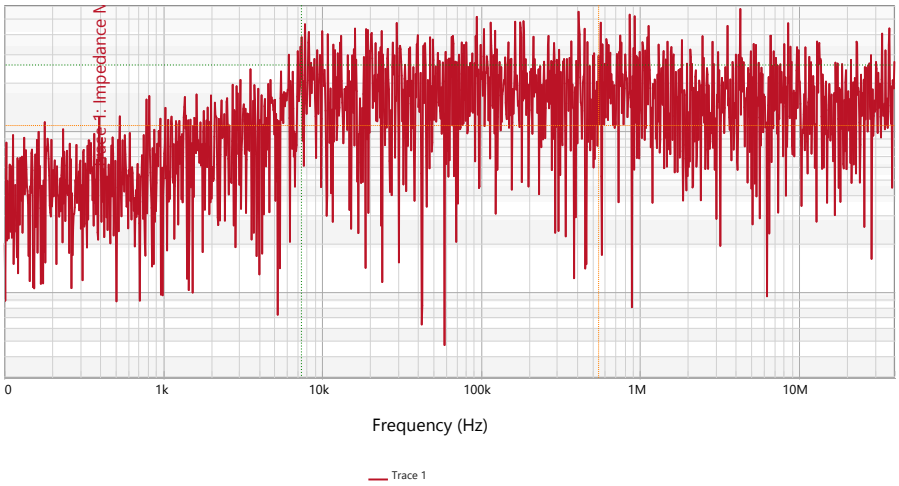




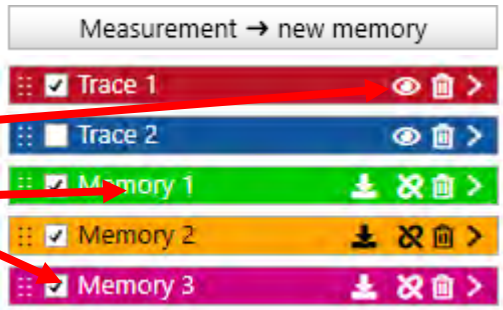




Results:

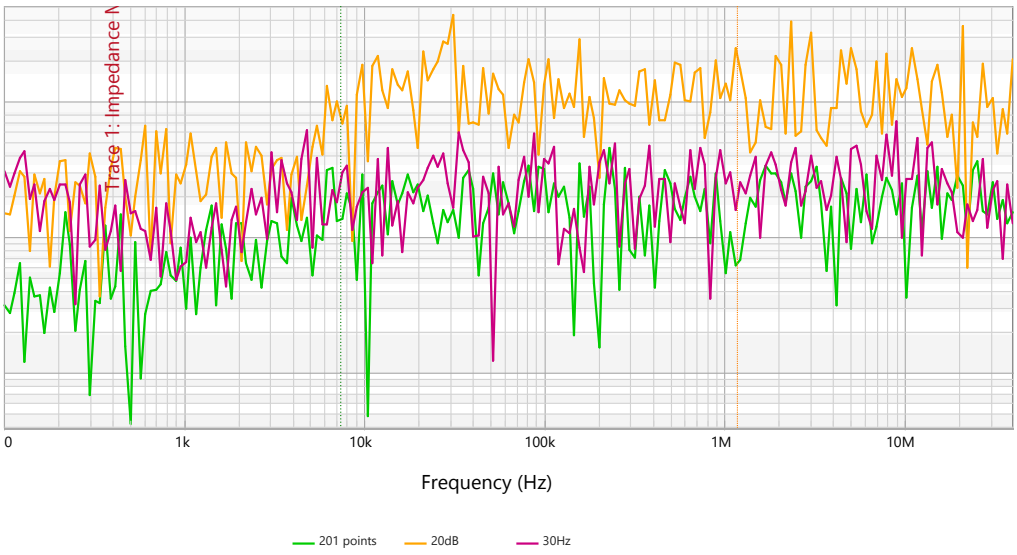


You can explore saving the waveform(s) to memory by clicking the **Measurement → new memory** button at the bottom right of the screen.



- You can toggle trace by clicking on the eye
- You can rename your memory traces by double clicking on the name.
- You can toggle a memory by unchecking the box.

The lower the resolution bandwidth the lower the noise floor. Addition of attenuation (attenuators) adds noise. These parameters are the main tools to reduce noise and generate a clean signal during a measurement.



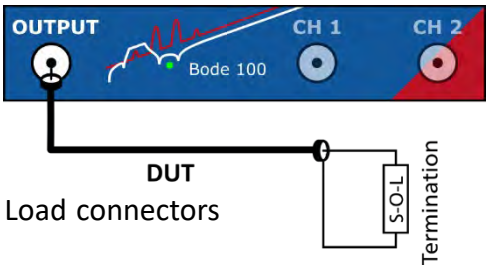
Hopefully, you are comfortable with the Bode 100 measurement software. We will be using the Bode 100 constantly to make these measurements, so it is important to familiarize yourself with the software, so you know what parameters to change or how to save your measurements. In addition, you now know the noise floor of your VNA so you know the limits of what can be measured using this instrument.

Cable Matching

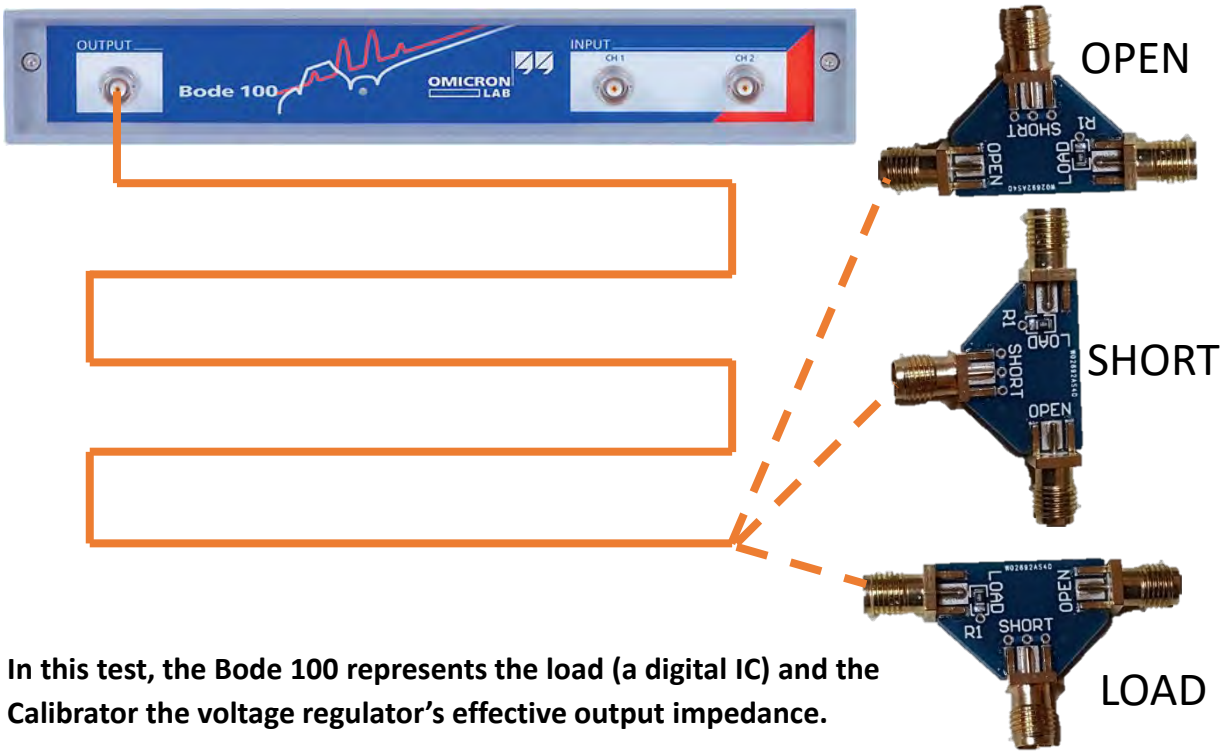
Description:
Cables and circuit board planes provide very flat frequency response when they are properly matched. When they aren't matched the cable or circuit board can be inductor or capacitive. Both conditions results in resonances that can significantly increase noise.

Measurement Setup:

1. File → New measurement → Impedance Analysis → One-port
2. Connect a **long** coax cable to the Bode 100 Output port
3. Connect the Open connector of the SOL calibrator to the other side.
4. Turn off Trace 2 by unchecking its check box.
5. Set the Start frequency to 10 kHz
6. Turn on Continuous measurement
7. Right click on the graph and select "Optimize"
8. Save the measurement to memory
9. Repeat the measurement with the Short and then Load connectors of the SOL calibrator
10. Save each sweep to a new memory location
11. Right click on the graph and select "Optimize"

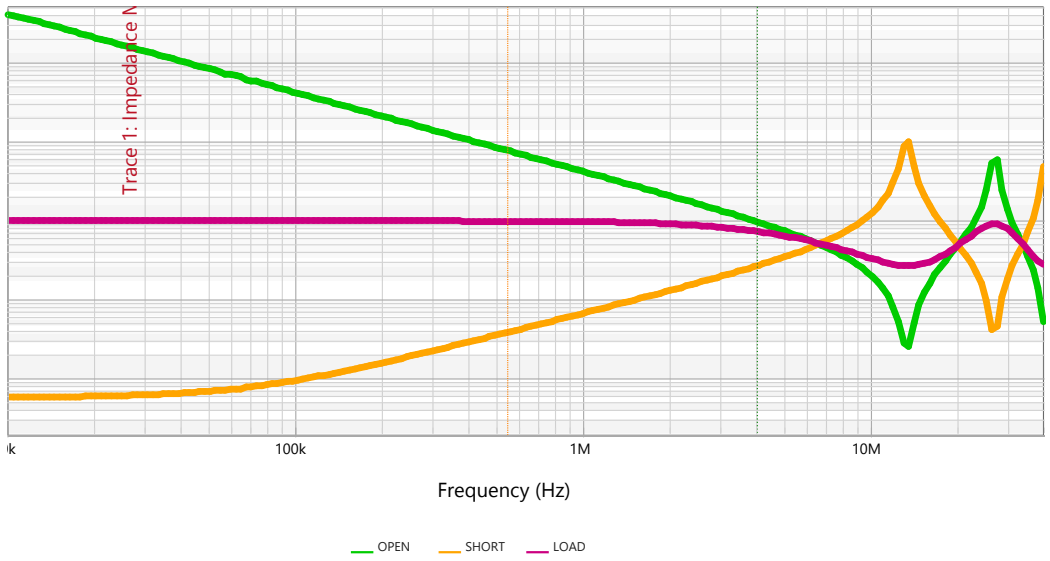


Setup Diagram:

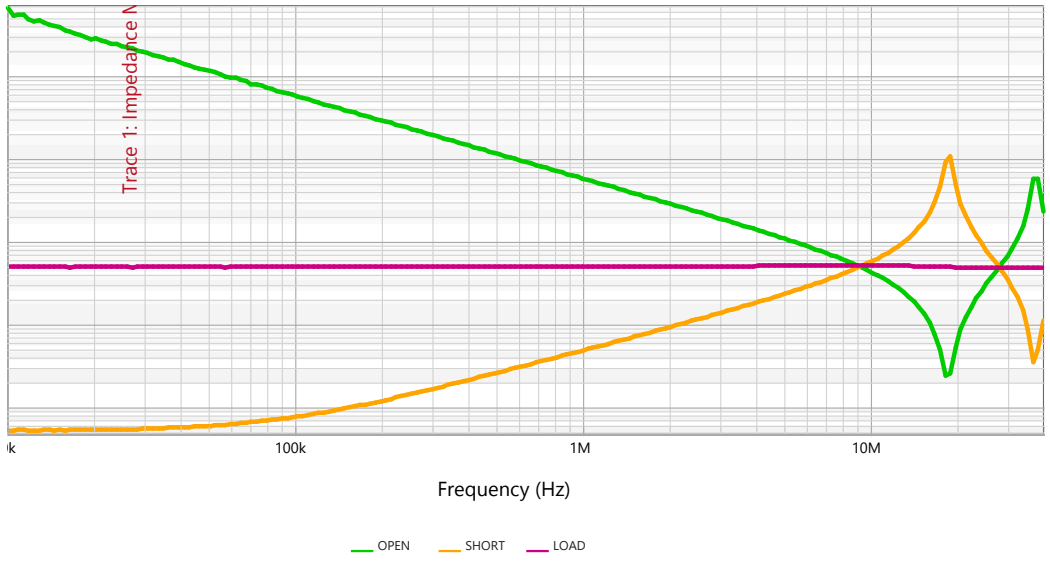


In this test, the Bode 100 represents the load (a digital IC) and the Calibrator the voltage regulator's effective output impedance.

Results:



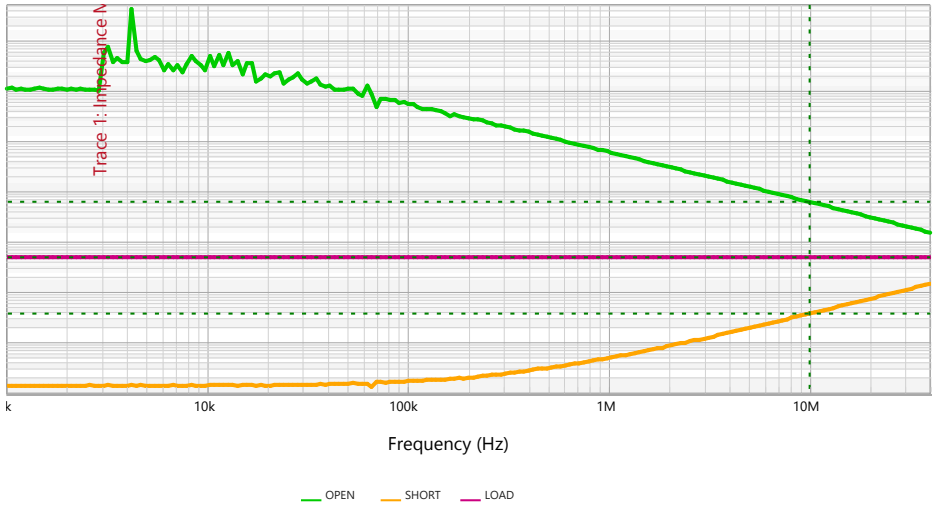
Note that the impedance is not flat. It is inductive or capacitive when unmatched. Two things need to match; the cable and either the DUT or the Bode100. Since the Bode100 is 50Ω and the load is 100Ω, it will not be matched.



The matched impedance response is flat. You must match the cable to the DUT or the instrument in order to get a matched flat impedance response. Here we have a 50Ω load which matched the 50Ω of the Bode100, thus measuring a flat impedance response.

Other things to Try:

- Measure a PCB Trace.



Note the impedance limit of about 100kOhms. The capacitive, inductive, and resistive responses apply equally to circuit board traces and cables. The matched impedance response is flat. We don't need to see the crossover impedance to determine the characteristic impedance or to know that the peaks will exist. We can see the higher frequency response of this trace when measured on a higher frequency VNA.

- We can calculate the balance point and characteristic impedance.

	Frequency	OPEN	SHORT	LOAD
Cursor 1	10 MHz	636.808 Ω	3.8 Ω	49.991 Ω

Calculation of Balance Point:

$$f_{bal} = f_{meas} \cdot \sqrt{\frac{OPEN}{SHORT}} = f_{meas} \cdot \sqrt{\frac{\frac{1}{\omega C}}{\omega L}} = f_{meas} \cdot \sqrt{\frac{1}{\omega^2 LC}}$$

Calculation of Z_0: $Z_0 = \sqrt{OPEN \cdot SHORT} = \sqrt{\frac{L}{C}}$

Note the open measurement is a capacitive measurement while the short is an inductive measurement. The characteristic impedance (Z_0) is ~50Ω. The balance point is ~130MHz.

Hopefully, after this experiment you can distinguish between a matched cable and an unmatched cable. Cable matching is crucial to having lower noise in the measurement. Before any measurement, be sure to check that your cables are matched by testing something you do know and verifying it. Remember, a flat impedance means that the cables are matched.

Measuring Impedance

Introduction:

Measuring the impedance of a device under test (DUT) is the most common and one of the most useful measurements. For individual components, the impedance can tell the individual characteristics of the component. We can then use that information to create accurate models for the components for simulations.

The measurement of low impedances can be difficult due to the limitations of various measurement techniques. The one-port reflection method is simple and allows the measurement of impedance above approximately 100mΩ up to over 2kΩ. With a probe, we can measure surface mount and header components. For through-hole components, we can also use the B-WIC impedance adapter to measure the impedance.

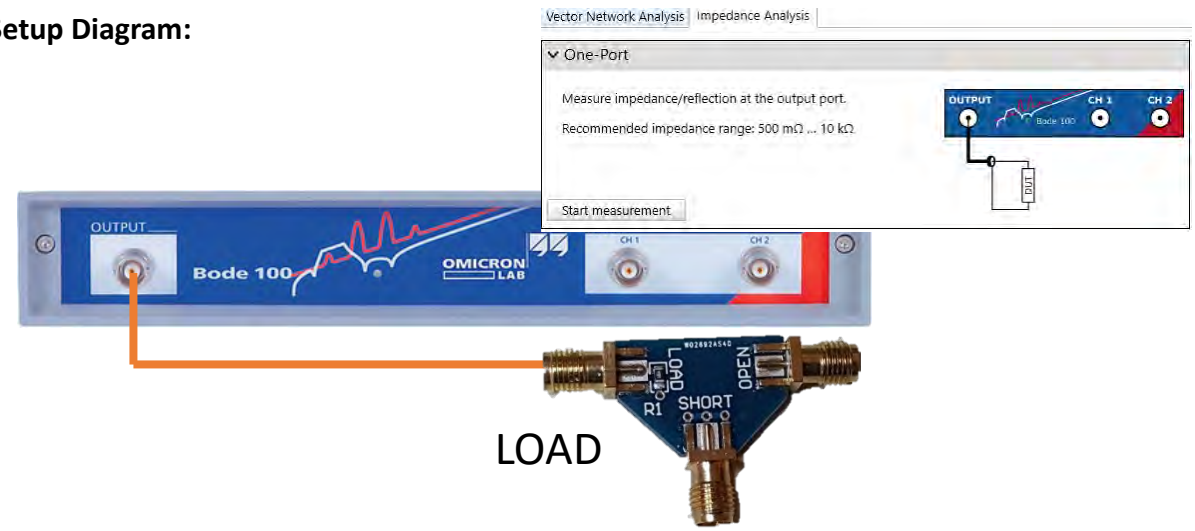
1-Port Reflection Measurement

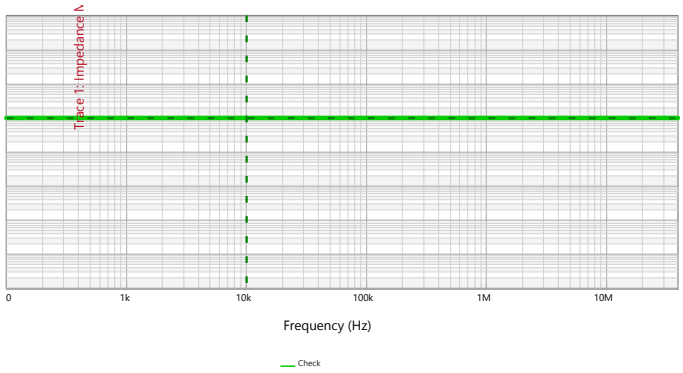
Making a 1-Port Reflection Measurement

1. Start a new 1-Port measurement by selecting Start measurement from the Impedance Analysis One-Port menu.
2. Or you can simply open the Bode 100 setup file: **1ohm_impedance.bode3.**
3. Connect a cable from the cable kit to the Bode 100 Output port via a BNC to SMA connector.
4. Perform the 1-Port SOL Calibration. **If your SOL Calibration board has a resistor other than 50ohms, click "Advanced Settings" and change the "Load Resistor" accordingly.**
5. After performing the calibration, leave the Load port of the calibrator connected. Turn off Trace 2 and start the Continuous sweep mode.
6. After confirming the resistor value, you can disconnect the SOL Calibrator and connect other components.

Always measure something you know to check your test setup and calibration. Best, if you check something of equal magnitude to the DUT that will be measured.

Setup Diagram:

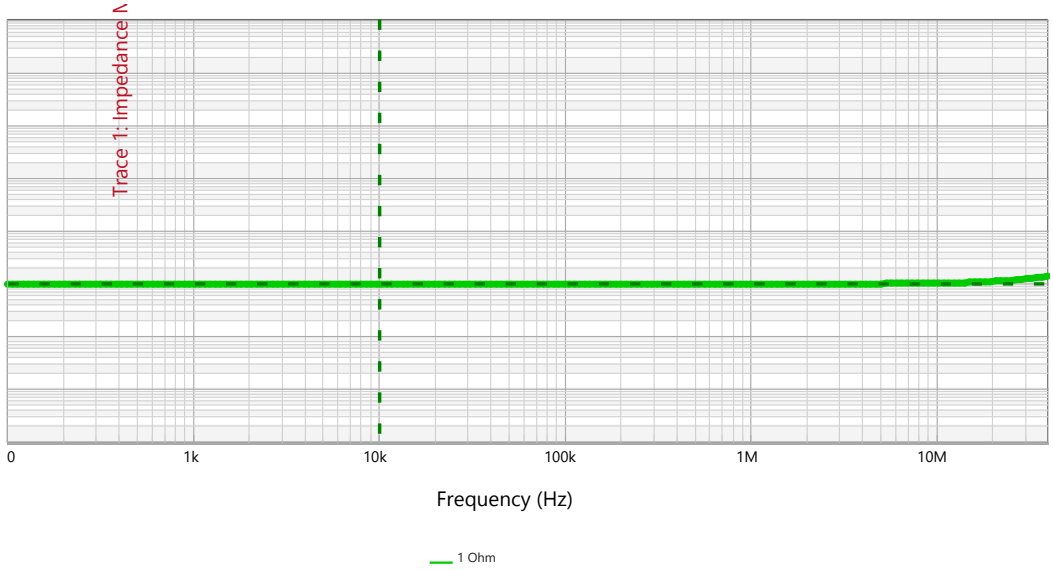




We will be measuring a 1Ω resistor so we can check our test setup and calibration with a 100Ω resistor. Notice that our check produces a flat line at 100. This means our setup is correct and calibrated properly

Hello World: 1 Ohm Measurement

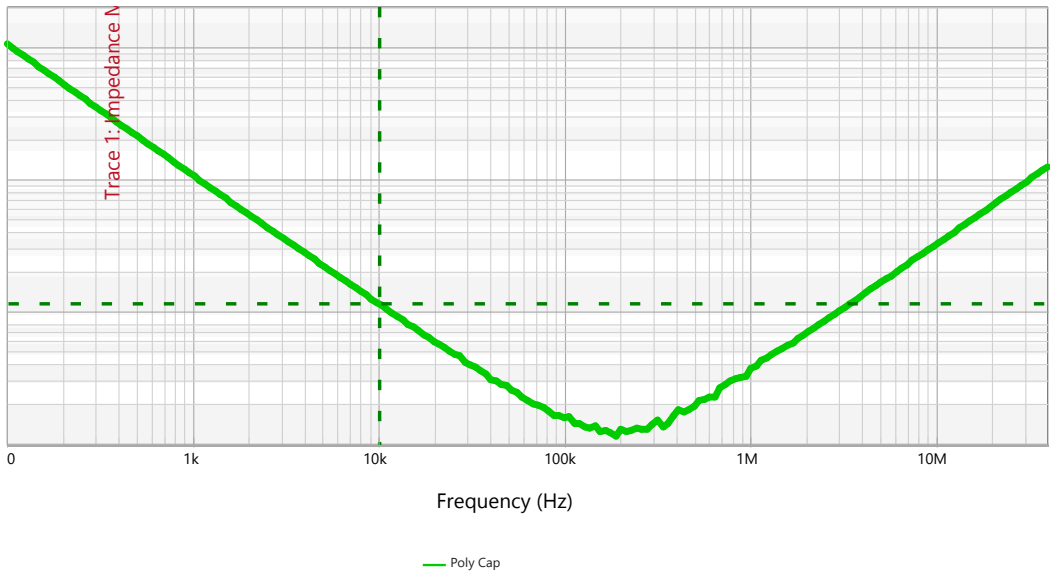
1. Connect a 1 Ohm resistor.
2. Right click on the graph and select Optimize to rescale the waveform.
3. Observe the flat impedance at 1 Ohm.



The rise at higher frequencies is due to the ESL of the resistor. All real-life resistors have ESL.

Other things to try:

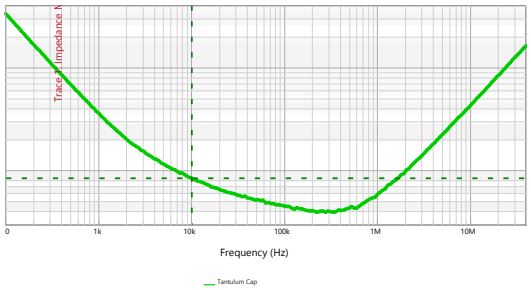
- Measure the Polymer Capacitor and notice the low ESR. You will need to Optimize the display in order to see the waveform.

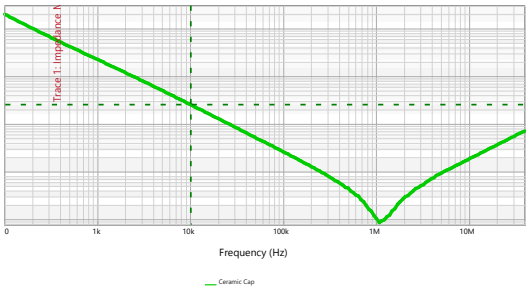


Notice the downward slope which represents the capacitance. Then levels off and hits 0 slope. This indicates the ESR of the capacitor. Then, the upward slope represents the ESL of the capacitor. With all three of these parameters, you can create an extremely accurate model for the polymer capacitor. This process can be done for any passive components.

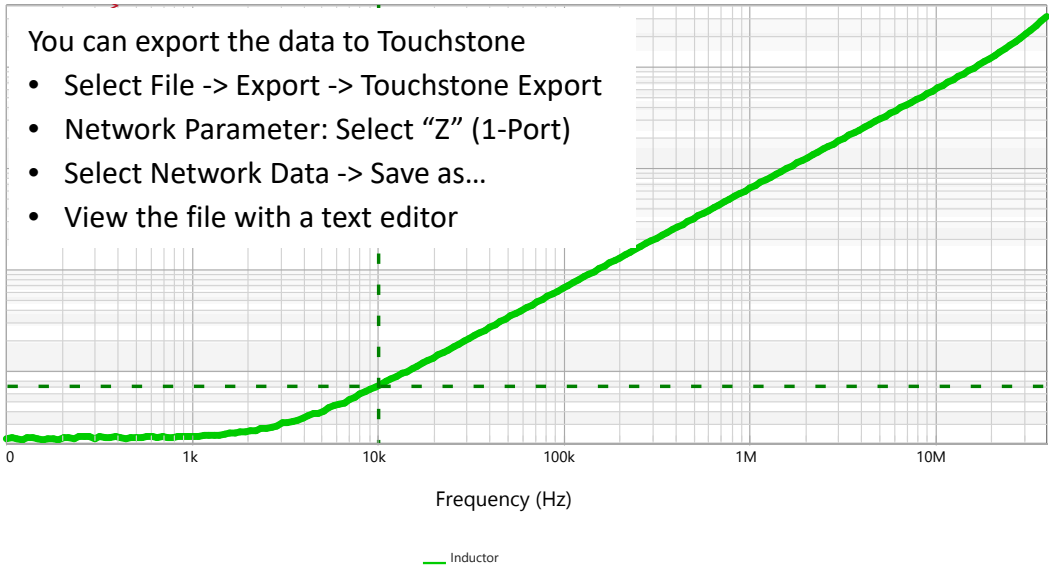
Other things to try:

- Measure a tantalum capacitor (left) and a ceramic capacitor (right). You will need to Optimize the display in order to see the waveform.

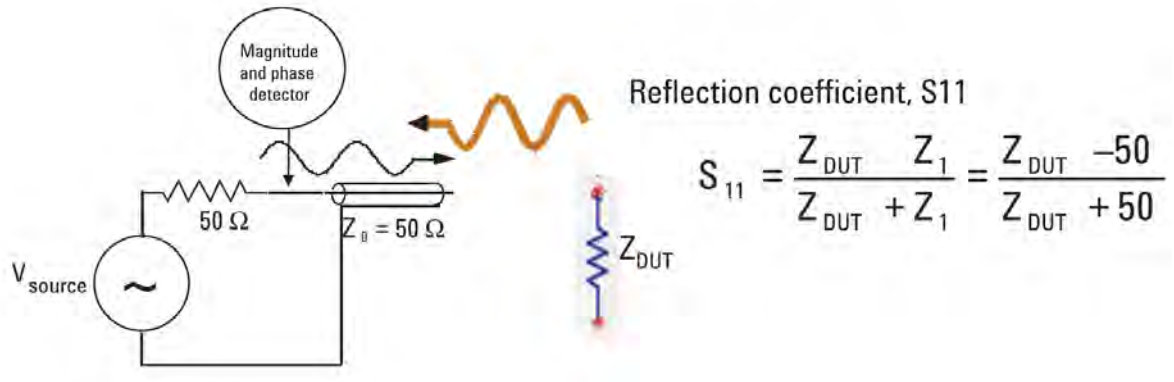




- Measure an inductor. You will need to Optimize the display in order to see the waveform. Take note of the flat region at low frequencies. This is the ESR of the inductor.



- If you were wondering how the VNA makes a measurement with one end not connected:



Hopefully, you now know how to make impedance measurements for resistors, capacitors, and inductors. This will allow you to model the components accurately. You should know how to calibrate for a one port impedance and how to verify that your setup is correct. You should know how to make a one port impedance measurement.

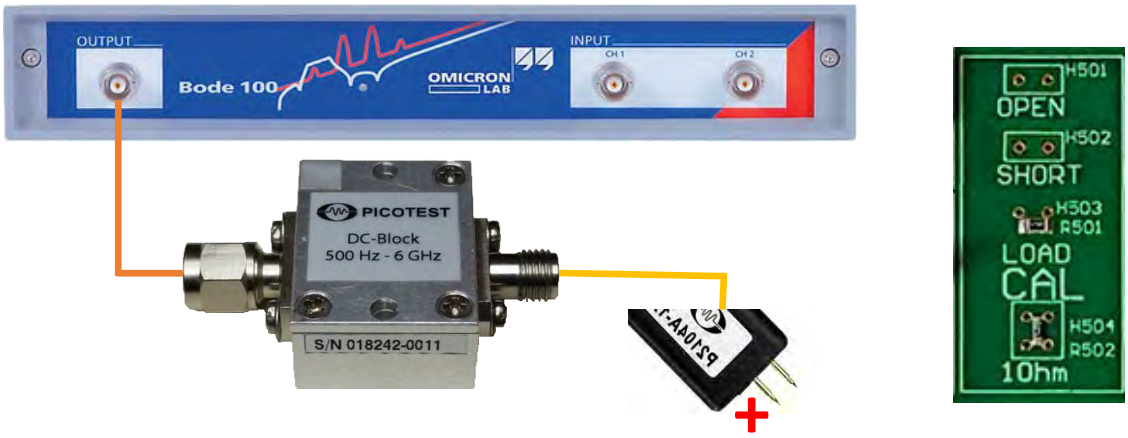
1-Port Probe Impedance Measurement

Description:
The output impedance of a voltage reference is a critical parameter in most distributed systems. Low noise depends on a flat impedance profile with a magnitude consistent with the needs of the circuitry being powered. As many circuits do not offer control loop access to assess stability, the output impedance offers a method of assessing stability as well. This test measures the output impedance of the REF03 voltage reference with and without an output capacitor using the 1-port reflection method.

Setup File: Open the setup file **1-port_z.bode3**
Calibration:

1. Connect the P2104A 1-port probe to the OUTPUT of the VNA through the P2130A DC block.
    - A P2130A DC Block is required to avoid loading the voltage regulator with the 50Ω from the probe.
    - The J2130A DC Bias Injector/Blocker can also be used.
2. Open a "One-port" impedance measurement.
3. Select "User-Range" or "Full-Range."
    - User-Range will calibrate the system to the parameters on the left side bar. This calibration is more accurate but will require re-calibration if parameters change.
    - Full-Range will calibrate the system to the full range of the system and interpolates the data in between. This is less accurate due to the interpolation but will not require re-calibration.
4. Locate and perform an OPEN-SHORT-LOAD calibration.
    - Polarity does not matter for calibration.
    - The LOAD calibration resistor on the VTS3 is 50Ω.
    - A 1Ω test resistor is provided to verify the calibration.

Remember to always measure something you know to check your test setup and calibration. Best, if you check something of equal magnitude to the DUT that will be measured.



1 Port Probe

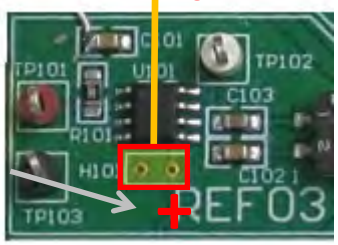
Instrument	Bode 100 VNA
Injectors	P2130A DC Blocker
Probe point	H101
Probes	P2104A 1-port probe (100 mil header)

Demo Board Settings:

S2-1	S2-2	S2-3	S2-4	S2-5	USB	S101-1	S101-2
OFF	OFF	OFF	OFF	OFF	ON	OFF	ON

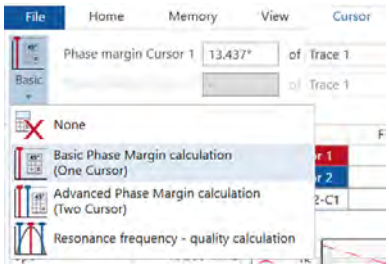
Setup Diagram:

1 Port Probe



Note the location of the plus sign and set the probe orientation accordingly

Same test using the J2130A DC Bias Injector/Blocker or P2130A Blocker

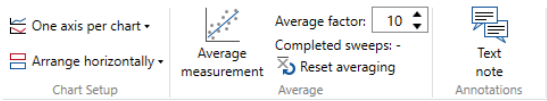


Measurement Steps:

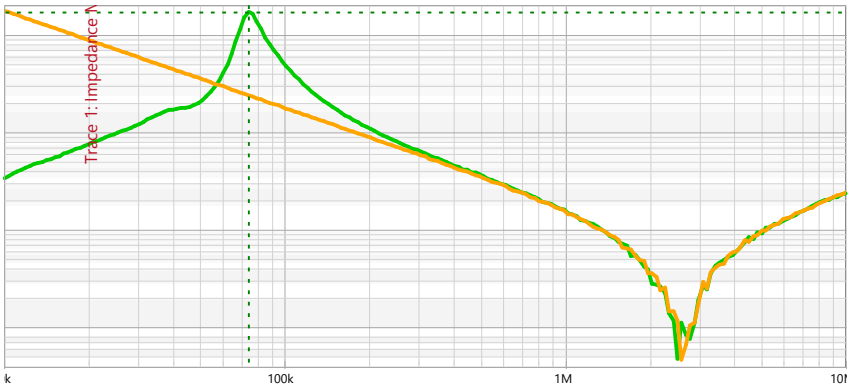
1. Make sure you are calibrated correctly.
2. Set the Format of Trace 1 to “Magnitude”.
3. Set the Format of Trace 2 to “Q(Tg)”.
4. Probe H101.
5. Disconnect the USB and take a OFF measurement.
6. Connect the USB and take a ON measurement.
7. Go to cursors and change the “Cursor Calculation” from “None” to “Basic”.
8. Place Cursor 1 at the Q(Tg) peak and record the phase margin.

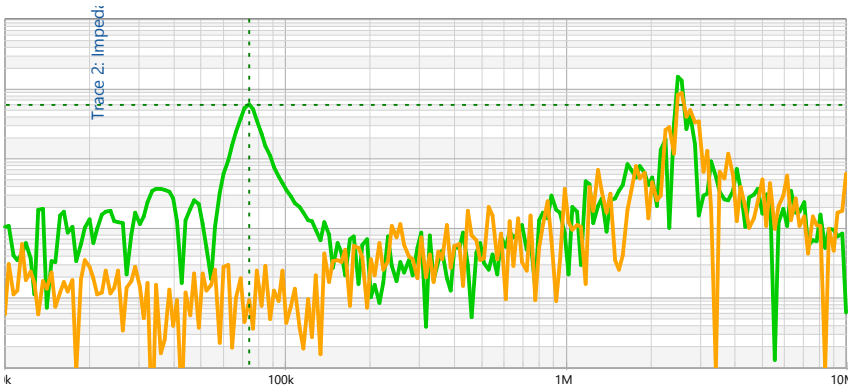
Tips:

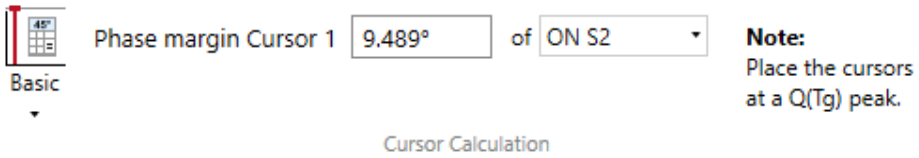
- Change the chart setup to “One axis per chart” to split up the traces. This will make it easier to find the Q(Tg) peak for the phase margin cursor calculation.
- Set the “Source Level” to a low number like -25 to -30 dbm. The source level needs to be low in order to see the impedance peaks.



Results:





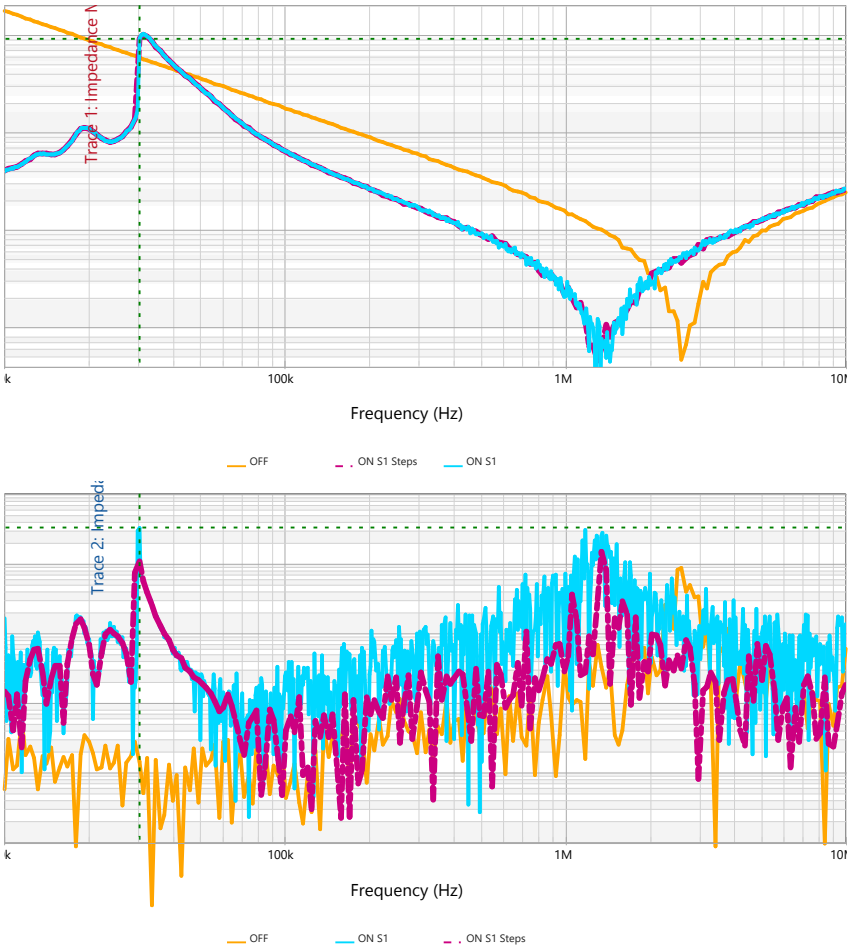


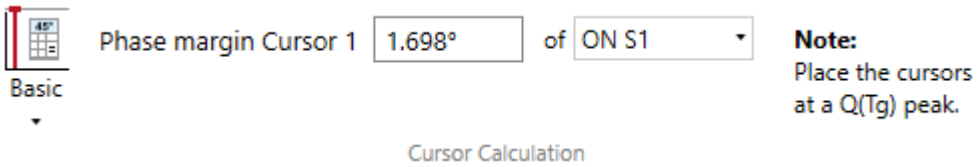
This is the output impedance of the voltage reference with a 0.33uF loading ceramic capacitor (Switch S101-2 ON). We measured the phase margin at the second Q(Tg) peak because that was the Q(Tg) peak closest to the impedance peak. The phase margin measured is ~9°. The source level being as low as possible at -30dBm shows the limitations of the 1-port probe measurement at low frequencies. We must have an ON measurement and an OFF measurement. NISM requires a peak when the power is on. With both states, we can determine which peak is the correct one to perform NISM. With both states, we can solve for the control loop

What is wrong with this measurement and why?

There is a peak at a frequency, therefore the power supply is oscillating. The peak is also not symmetrical. Being asymmetrical signifies a bad measurement as the source injection level is too high for the circuit and the Bode 100 to measure even though we set it to its lowest injection level (-30 dbm). The signal is too large which forces the circuit to operate in a nonlinear region.

Other things to try:





This is the output impedance measurement of the voltage reference with a 0.1uF loading ceramic capacitor (Switch 101-1 ON). Notice the decrease in phase margin as we increase the capacitive loading. Notice how the peaks are even more asymmetrical. This means that we are overloading the measurement even more than before and, therefore, cannot make an accurate measurement.

Also, notice the purple trace. The peak in the Q(Tg) graph was not very smooth. This means that the number of points was too small. There are two ways to fix that. One is to increase the number of points. That is what is shown in the Cyan trace. We increased the number of points to 801 points. The second way is to limit the range. If we zoomed in on that peak and ran another measurement, the Bode software would measure 201 points in that zoomed in range. As we can see, the Q(Tg) peak has changed and is more defined. This also gave us the phase margin of ~2°.

We added some attenuation using the J2140A Attenuator. We added 10dB of attenuation. This gave us more symmetrical peaks which means we lowered the source injection level enough.

Hopefully, now you know how to measure the output impedance of a voltage reference and determine its phase margin. You should also be comfortable with calibrating a 1-port probe and how to verify your setup and calibration.

Additional Resources (Power Integrity, pages 109-122):
https://www.picotest.com/blog/?p=1307 – Trouble Shooting Distributed Power Systems Video

Impedance Adapters

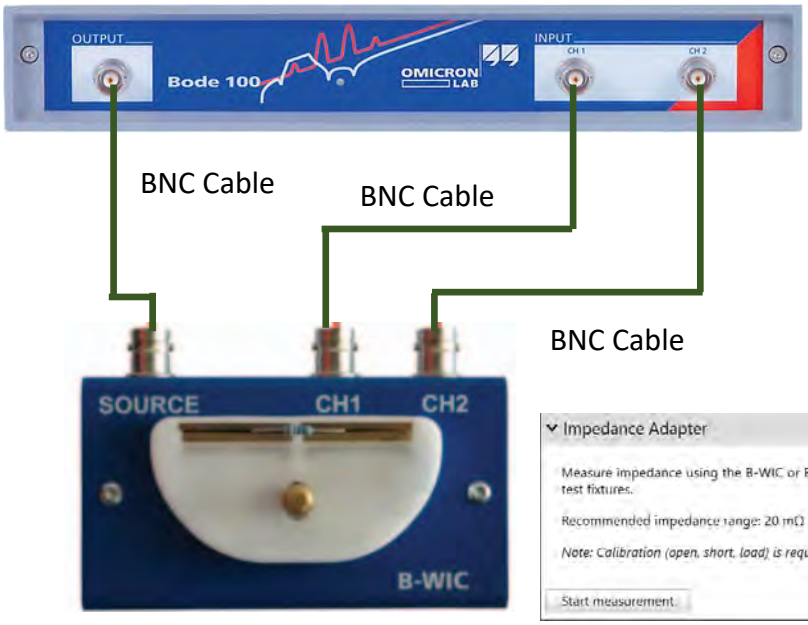
Description:
The ESR of a capacitor is an important parameter that has a significant influence on the behavior of power supplies. The impedance adapter allows for easy impedance (ESR, ESL, DCR, etc.) measurement of through-hole components. This test measures the ESR and capacitance of a capacitor over a frequency range and then explores the different plotting formats available in the Bode 100.

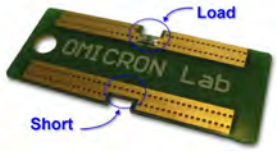
Instrument	Bode 100 VNA
Injectors	B-WIC Impedance Adapter
Probe point	N/A
Probes	N/A

Setup file: Open the setup file **impedance adapter.bode3**
Calibration:

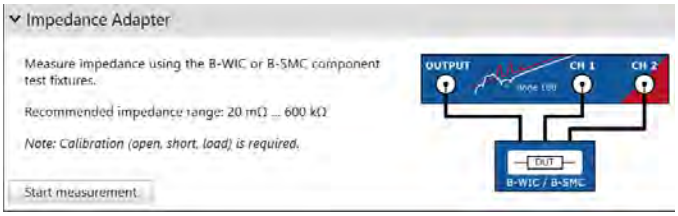
1. Connect the impedance adapter to the Bode100 as shown in the setup diagram and select “Impedance Adapter” measurement
2. Perform an OPEN-SHORT-LOAD calibration using the B-WIC calibration board.
3. Do not insert anything into the Impedance Adapter when performing an Open calibration.
4. Insert the short side of the calibration board when performing the Short calibration.
5. Insert the load side of the calibration board when performing the Load calibration.
6. Measure the impedance of the 100Ω LOAD calibration resistor. A proper calibration should result in the correct measurement of the LOAD calibration resistor.

Setup Diagram:



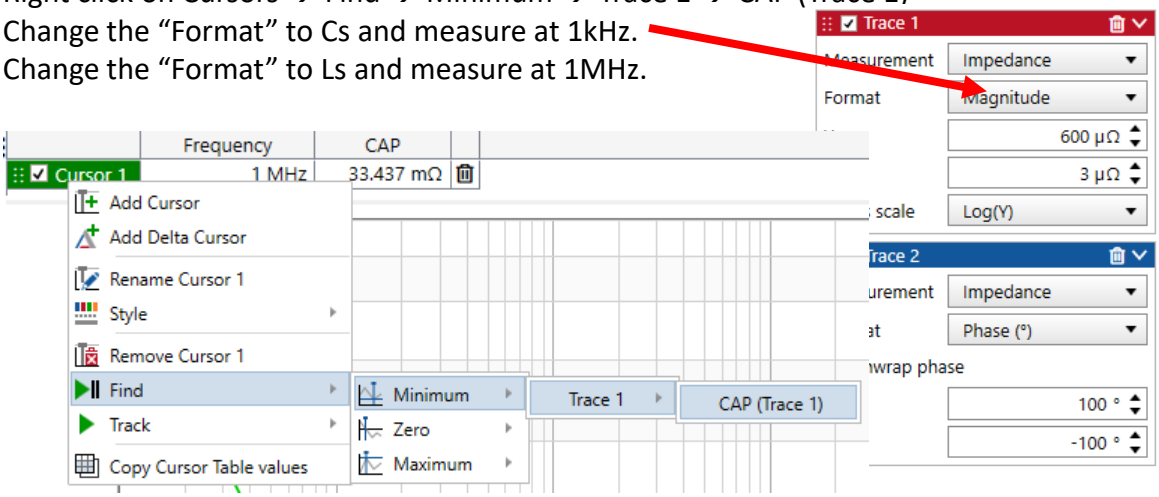


B-WIC calibration board

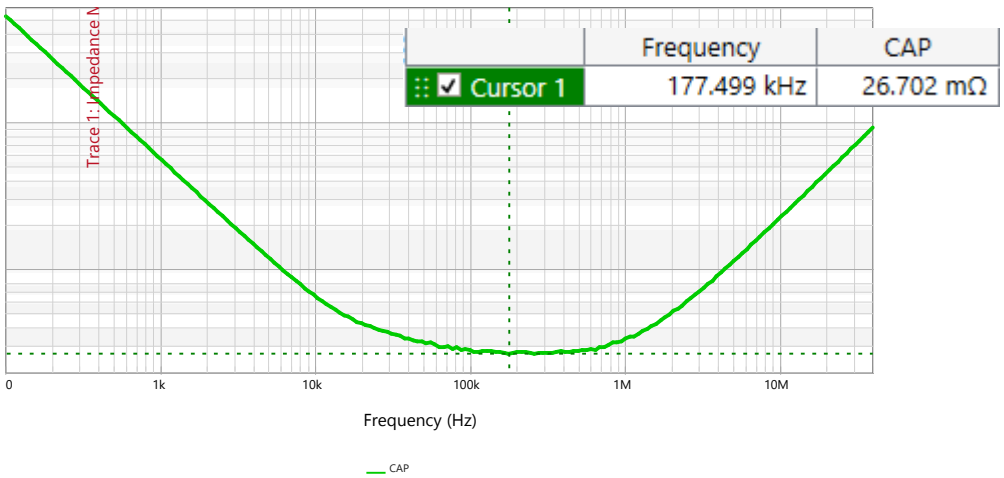


Measurement Steps:

1. Replace the calibration board with the 330µF 35V through-hole capacitor.
2. Turn off Trace 2 by unchecking the Trace 2 box.
3. Measure the Impedance Magnitude.
4. Right click on Cursors → Find → Minimum → Trace 1 → CAP (Trace 1)
5. Change the "Format" to Cs and measure at 1kHz.
6. Change the "Format" to Ls and measure at 1MHz.

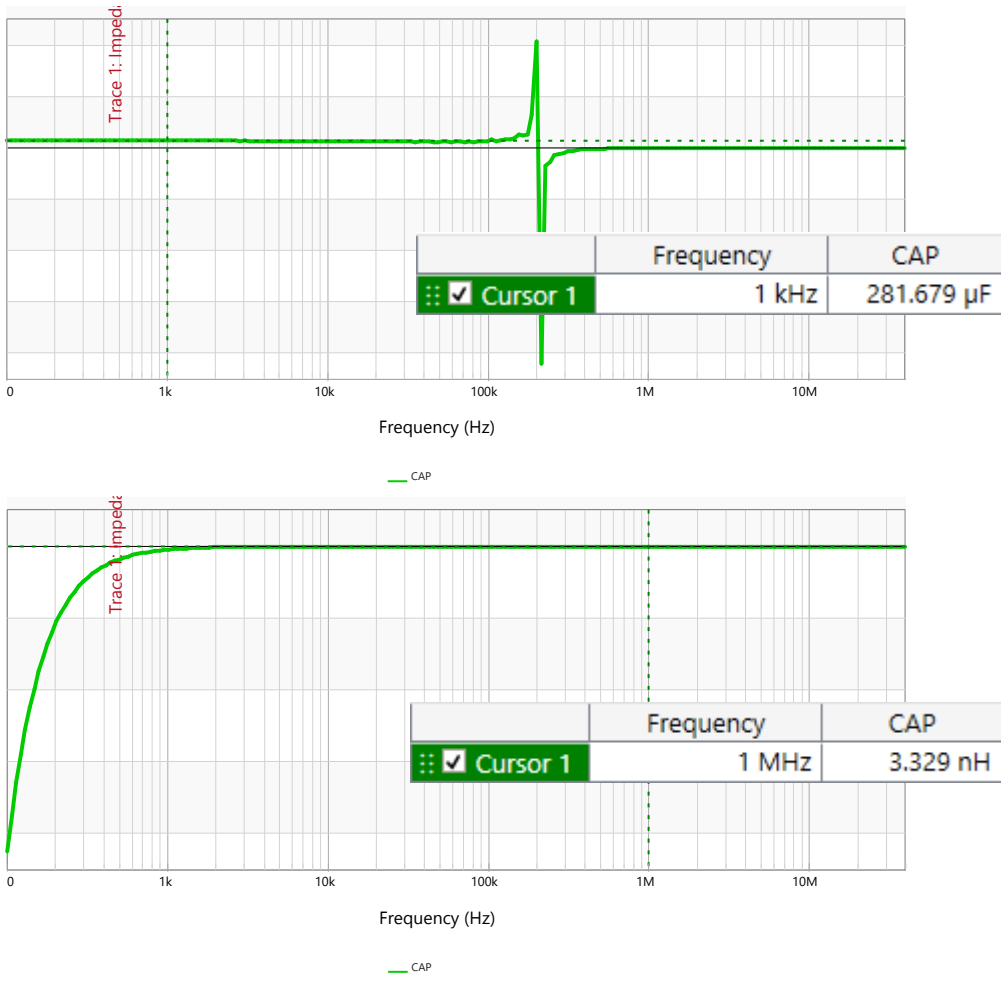


Results:



This is the impedance graph of a 330µF 35V through-hole capacitor using the B-WIC Adapter.

You can change the format of the output at anytime during the measurement. In this experiment, change the format to Cs (series capacitance) and Ls (series inductance). Then we can use cursors to determine the value for these parameters.



Other things to try:

- If the datasheet specifies an ESR value at a certain frequency, compare the datasheet value with the measured value
- Repeat the measurement with a different capacitor from the same bin in order to observe its ESR range.

Hopefully, this experiment taught you how to use the B-WIC impedance adapter. This adapter useful for through-hole components or components that cannot be easily connected with cables. You should also be comfortable with the different measurement formats the Bode 100 offers. You should be able to change the settings to the desired measurement and record the necessary numbers to create accurate models for simulations.

Additional Resources (Power Integrity, pages 142-148):

http://www.omicron-lab.com/fileadmin/assets/application_notes/App_Note_ESR_Measurement_V1_2.pdf
http://www.omicron-lab.com/fileadmin/assets/application_notes/DC_Biased/App_Note_DC_Bias_Impedance_V1_1.pdf

Measuring Power Systems

Introduction:

Now that we know how to measure the impedance of components and how to use the 1-port probe, we can extend the same measurement to power systems. We already used the 1-port probe to measure the output impedance of the voltage regulator. We can extend the 1-port probe impedance measurement to many other power systems, like a point of load (POL) or opamp power circuits. We already showed that we can get the phase margin from the impedance measurement. The 1-port impedance will have its limitations at low impedances but can still be used to get a good sense of the power system's stability. We will also conduct the measurement under different loading conditions to see how capacitors and other loads affect the impedance and ultimately the stability of the power system.

POL Output Impedance

Description:
The single port impedance reflection measurement can give distorted results at low impedances. This limits its usability. However, it is very useful for quickly assessing stability problems in low power circuits across an entire card. This test measures the impedance and stability of a point of load (POL) regulator under different loading conditions.

Instrument	Bode 100 VNA
Injectors	N/A
Probe point	H5
Probes	P2104A 1-port probe (100 mil header)

Setup file: Open setup file **pol_out.bode3**
Measurement Steps:

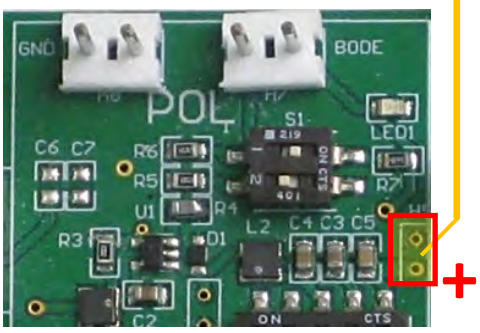
1. Connect the P2104A 1-port probe to the OUTPUT of the VNA.
    - A P2130A DC Block is not required because we are not loading any components and our voltage levels will not be above 3.3V.
2. Open a “One-port” impedance measurement.
3. Perform a SOL calibration.
4. Probe H5.
5. Trace 1 is “Magnitude” and Trace 2 is “Q(Tg)”.

Demo Board Settings:

S2-1	S2-2	S2-3	S2-4	S2-5	SEL1	USB	S1-1	S1-2	S401-1	S401-2
OFF	OFF	OFF	OFF	OFF	LEFT	ON	ON	OFF	OFF	OFF

Setup Diagram:

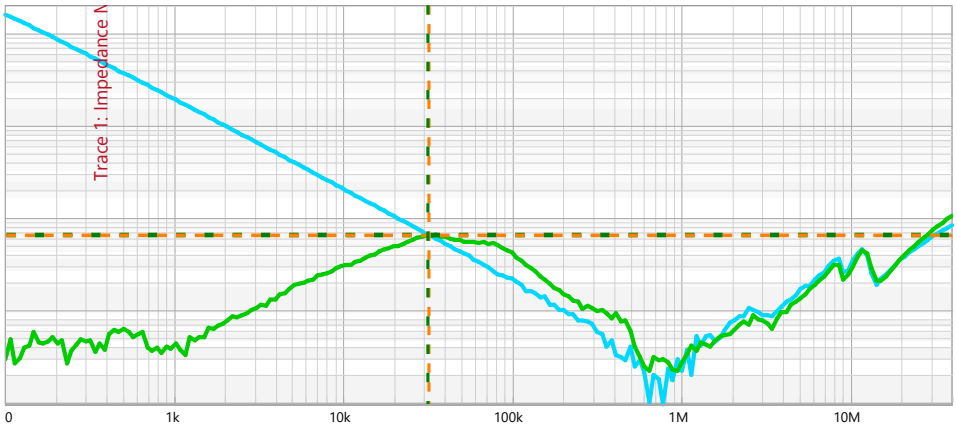
BNC to SMA Connector

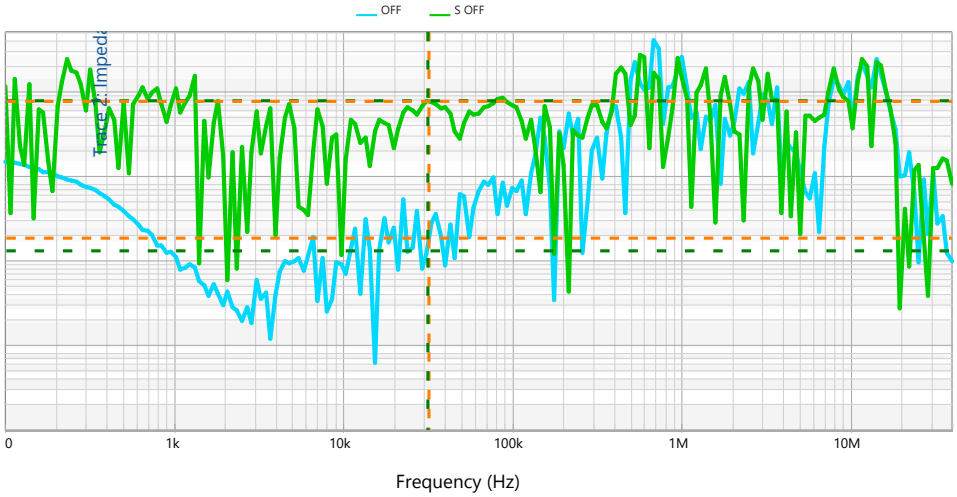


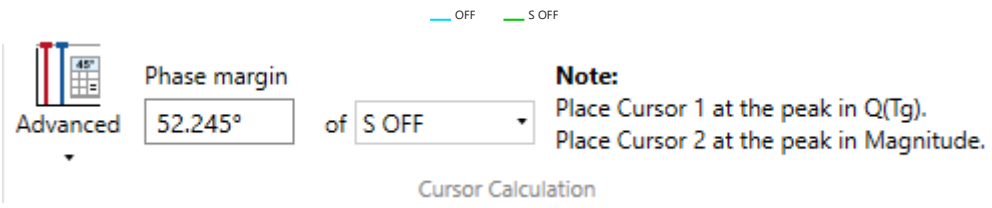
1 Port Probe

Note the location of the plus sign and set the probe orientation accordingly

Results:



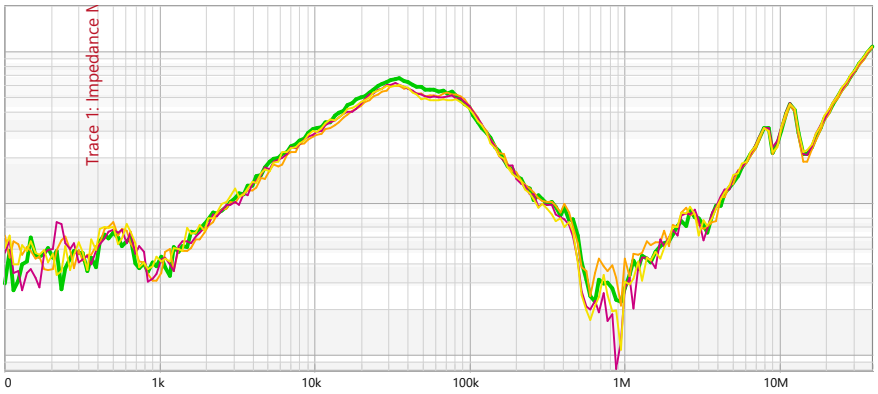


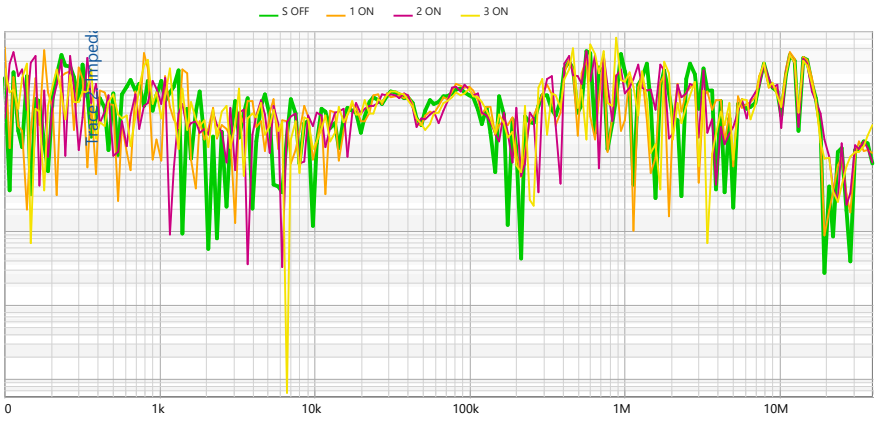


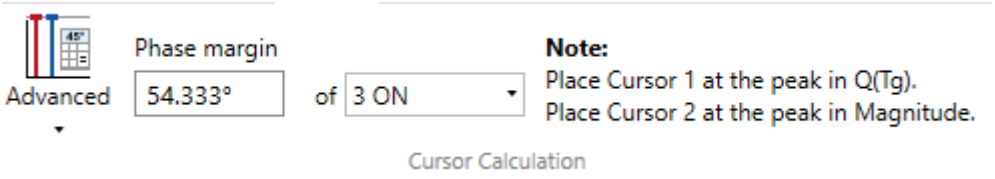
We do measure a peak. We can then do another phase margin calculation. This time use the "Advanced Phase Margin Calculation". Place cursor 1 at the peak of the Q(Tg) graph and place cursor 2 at the peak of the Magnitude graph. We measure a phase margin of 53.245° which is way above the 30° threshold required by most analyses. However, notice that the peak is wide and not a sharp and symmetrical peak. This is because the 1-port measurement is limited at low impedances.

Let's see what happens when the POL experiences different loading conditions. We will do this by switch on and off S2-3, S2-4, and S2-5. Each switch will increase the load by 33Ω and thus increase the output current.

Results:







As we increase the loading of the POL, the output impedance does not change very much. This is because the 1-port measurement is limited at low impedances. The phase margin is also maintained as we increase the loading. Even with all three switches ON, which is the greatest loading that can be achieved, we still maintain 54°.

Hopefully, you can measure the output impedance of a POL regulator. You should also experience the limitations of the 1-port probe at low impedances. You now know how to use the “Advanced” phase margin calculation. You should have a better idea of how loading the POL affects its output impedance.

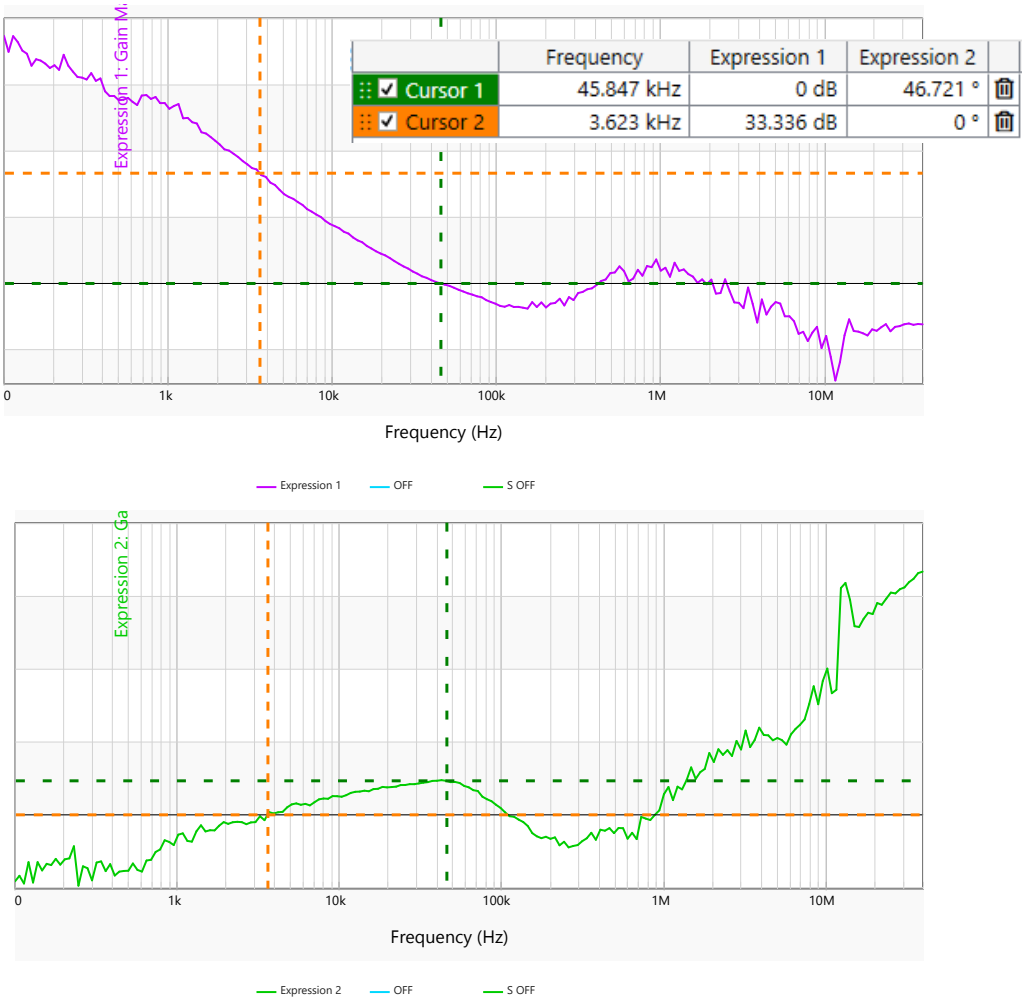
Additional Resources (Power Integrity, pages 109-122):
http://powerelectronics.com/regulators/assessing-point-load-regulators-using-non-invasive-techniques

Other Things to Try:

Now that we have the output impedances, we can also derive the bode plots from these results.

Math Expression Steps:

1. Measurement → Add expression
2. Use the "Trace Values" to access the measurements.
3. For Magnitude, enter the expression "(Z{OFF}/Z{S OFF})-1"
4. For Phase, enter the expression "1-(Z{OFF}/Z{S OFF})". The expression is different to move the phase plot down by 180°



Using the Bode100 software, we can plot the bode plot from the measurements. We can then measure the phase and gain margin. The phase margin from the bode plot is ~46° which is comparable to the NISM result of ~52°. From the output impedance measurement, we can derive the bode plot. The output impedance measurement is a better and more useful measurement.

Opamp Output Impedance

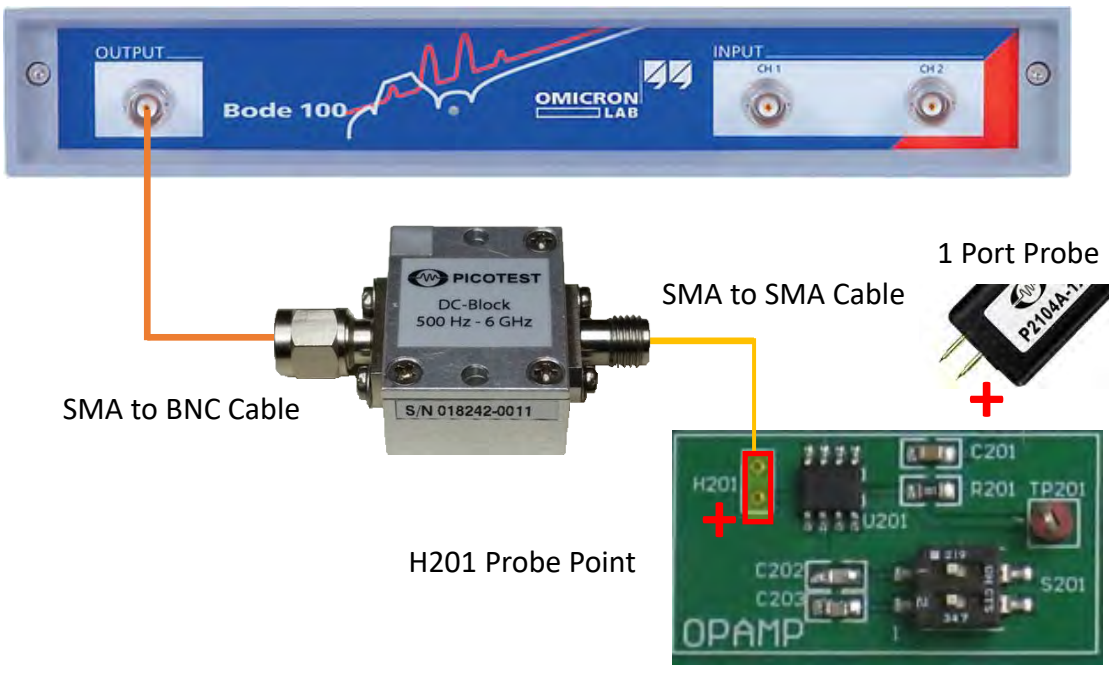
Description:
This test measures the output impedance and the corresponding group delay of an opamp buffer. The change in the stability response is analyzed for different loading capacitances.

Instrument	OMICRON Lab Bode 100 VNA
Injectors	P2130A DC Blocker
Probe point	H201
Probes	P2104A 1-port probe (100 mil header)

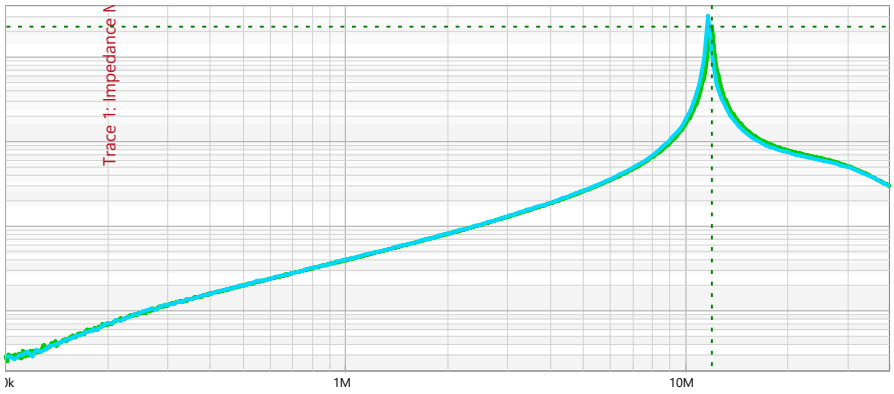
Setup file: Open the setup file **opamp.bode3**
Measurement Steps:

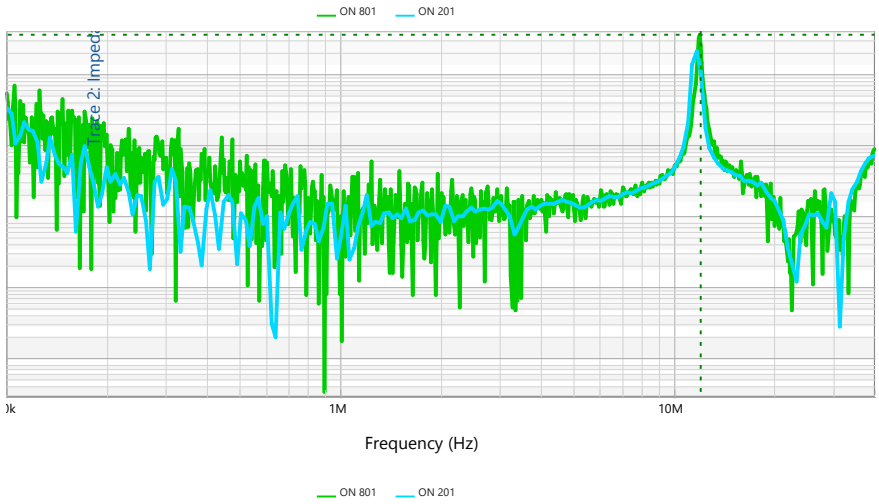
1. Connect the P2104A 1-port probe to the OUTPUT of the VNA through the P2130A DC block.
    - A P2130A DC Block is required to avoid loading the opamp with the 50Ω from the probe.
    - The J2130A DC Bias Injector/Blocker can also be used.
2. Open a “One-port” impedance measurement.
3. Perform a SOL calibration.
4. Probe H201.
5. Trace 1 is “Magnitude” and Trace 2 is “Q(Tg)”.
    - The source level needs to be very low to see the results.

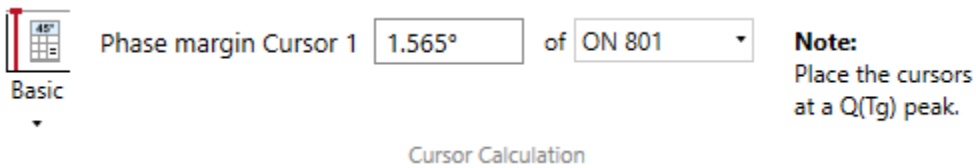
Setup Diagram:



Results:



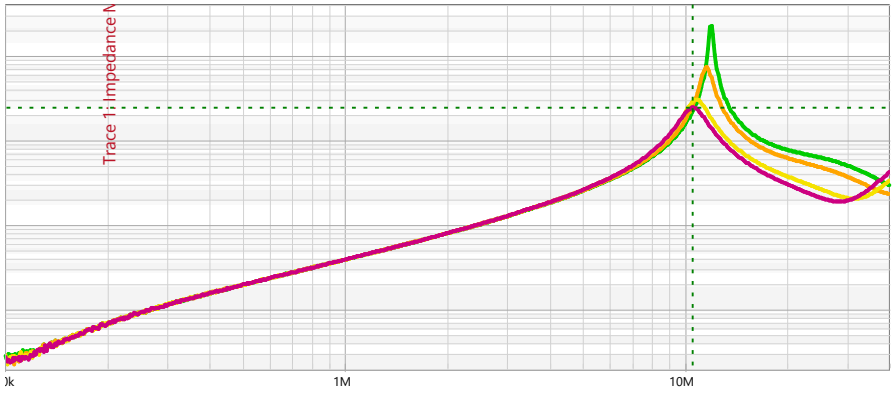


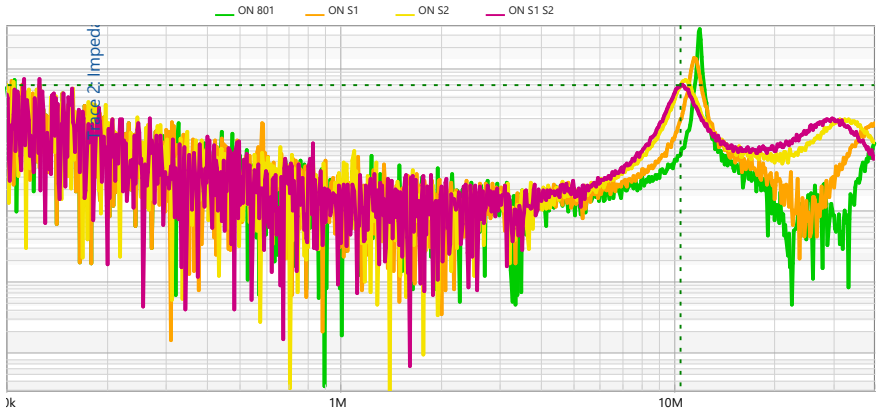


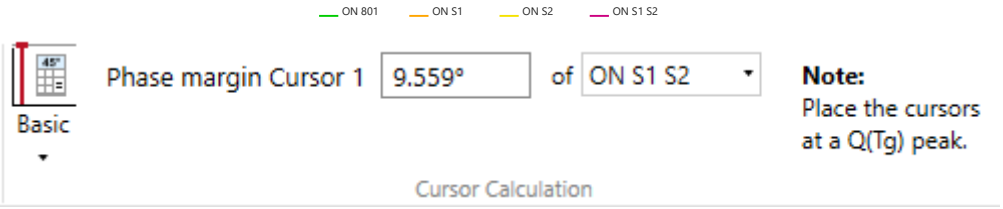
We perform the same measurement as the voltage regulator measurement. We did have to increase the number of points to 801. This is because the peak in the Q(Tg) graph was not well defined. We did not have enough points to see the peak. We also measure the phase margin. The phase margin was ~1°.

Let's see if increasing the capacitive loading will help with the phase margin and ultimately the stability. We will be switching the switches on S201 to increase the capacitive loading and making the same measurement.

Other things to try:







As we increase the loading the opamp with more and more capacitors, the peak increases and the phase margin decreases. Since lower phase margin leads to larger Q, the stability of the signal becomes poorer. It seems like increasing the capacitive loading makes the phase margin worse. The source level being as low as possible at -30dBm shows the limitations of the 1-port probe measurement at low frequencies.

Hopefully, you know how to measure the output impedance of an opamp buffer. You should also be able to get a good sense of the performance and stability of the opamp through the measurement.

Additional Resources (Power Integrity, pages 109-122):
https://www.picotest.com/blog/?p=864 - Introduction to the J2110A Solid State Injector

Distributed Power Systems

Introduction:

The step load response is another crucial test for power systems. First, like most other tests, it can assess the stability of the control loop. The measurement will not produce a direct phase margin number but there is a direct relationship between the oscillations in response to a step load and its phase margin. Another useful result is the overshoot and/or undershoot that happens in response to a step response. The response to a step usually has the highest peaks or lowest valleys for voltages produced. Sometimes this is necessary to know for certain components that only work within a certain operating range. We do not want to break or degrade components and a step load response can tell us to what extent the voltage changes. The step load response also gives us the large signal behavior and how it can affect other circuits that use this same power rail.

The step load response gives a qualitative description of the power rail. It can give both large and small signal responses that is important to know. In these experiments, we will be using a current injector to generate the step load. Make sure that the impedance of the load does not influence the measurement. We will look at that in **Edges Example – Different Probes**. We will then observe how to measure the step load response with a one-port probe and additionally, how to measure the response with a two-port probe. We will measure the Step Load of **Voltage Reference** and **LDO Regulator**.

Edges Example-Different Probes

Description:
The type of probe used to measure an edge may have a significant impact on the fidelity of the measurement. A 1X probe does not attenuate the measured signal, however the load capacitance of the probe is higher than a 10X probe. A 10X voltage probe, which introduces attenuation to the signal, will have a lower capacitive load at the expense of a higher minimum measurable signal. This test measures the rising edge of the 10MHz clock signal using a 1X and 10X probe.

Instrument	Oscilloscope
Injectors	NA
Probe point	TP402, TP403
Probes	1:1 probe, 10:1 probe

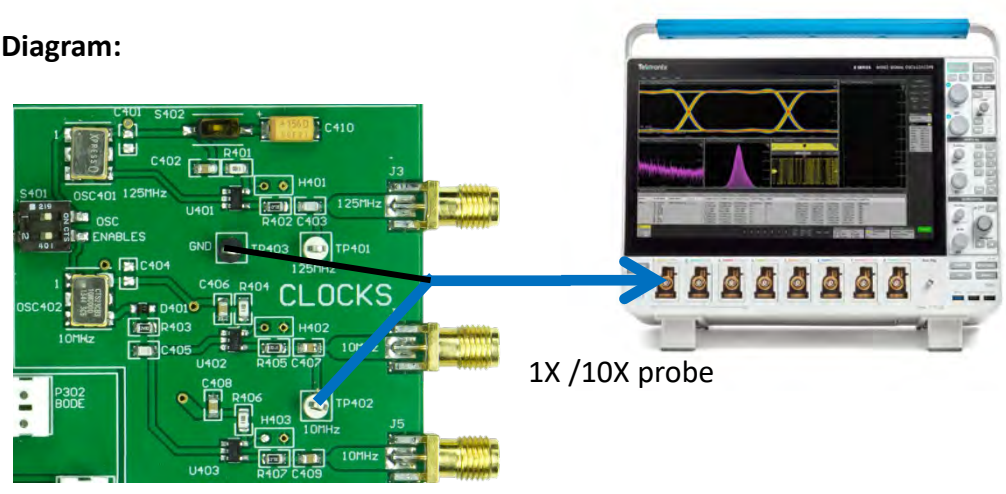
Setup file: Open the setup file **edge.tss**
Measurement Steps:

1. Plug the USB into the VRTS3P3 board.
2. Set the Switch (SEL1) to the right and set S401-1 and S402-2 in their off position (Left).
3. Connect the voltage probe to CH1 of the oscilloscope.
4. Connect your voltage probe to TP402 and the ground pin to TP403.
5. Set the Impedance of CH1 to 1MΩ DC.
6. CH1 should show a 10MHz clock signal.
7. Set the probe attenuation to 10:1 and repeat the measurement for a 10X probe.
8. Measure the rise and fall time of the CLK signal.

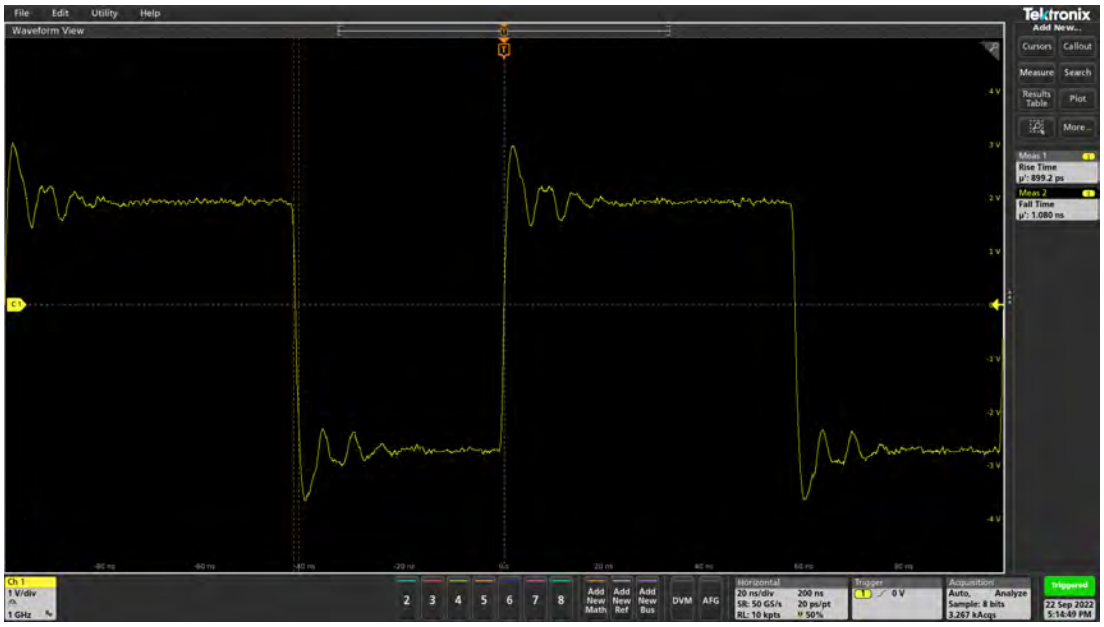
Board Settings:

SEL1	USB	S401-1	S401-2
RIGHT	ON	OFF	OFF

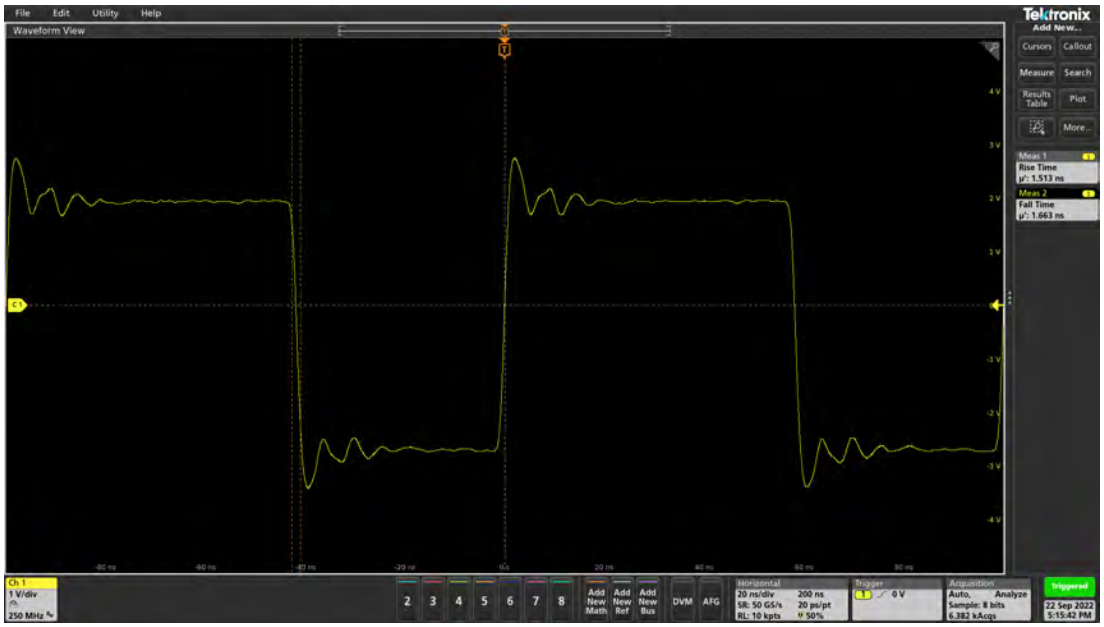
Setup Diagram:



Results:



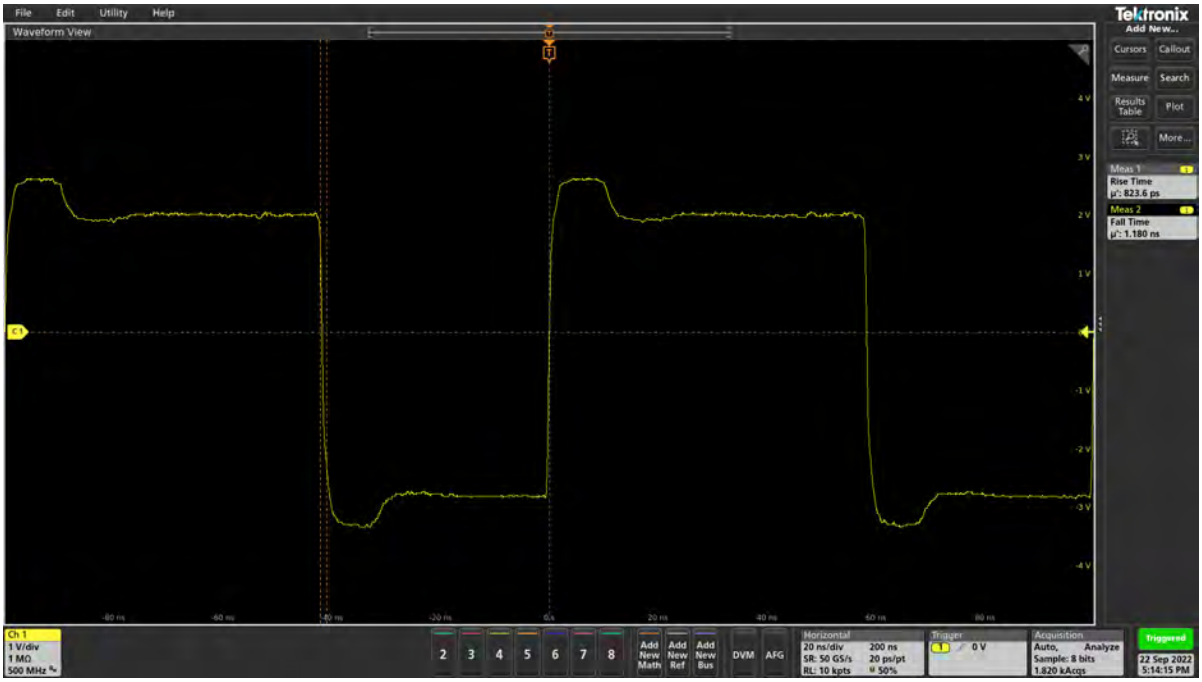
Measurement using the TP1000 Probe



Measurement using the TP1000 Probe at a different sampling rate (250MHz)

Other Things to Try:

- Connect the J4 of the VRTS3P3 directly to the scope.



- Compare the rise and fall time of all three measurements.

Measurement	Rise Time (ns)	Fall Time (ns)
1GHz Probe (Sampling Freq: 1GHz)	0.8992	1.080
1Ghz Probe (Sampling Freq: 250MHz)	1.513	1.663
50Ω Cable (Direct Connection)	0.8236	1.180

Hopefully, you now know how different probes and different kinds of probes can affect the measurement. Each probe is unique and presents its own set of noise. Make sure you pick the correct that suit your measurement needs.

Additional Resources (Power Integrity, pages 269-273):

https://www.picotest.com/blog/?p=1387 - Oscilloscope Mistakes: #2 (Part 2 of 4)

Voltage Reference Step Load

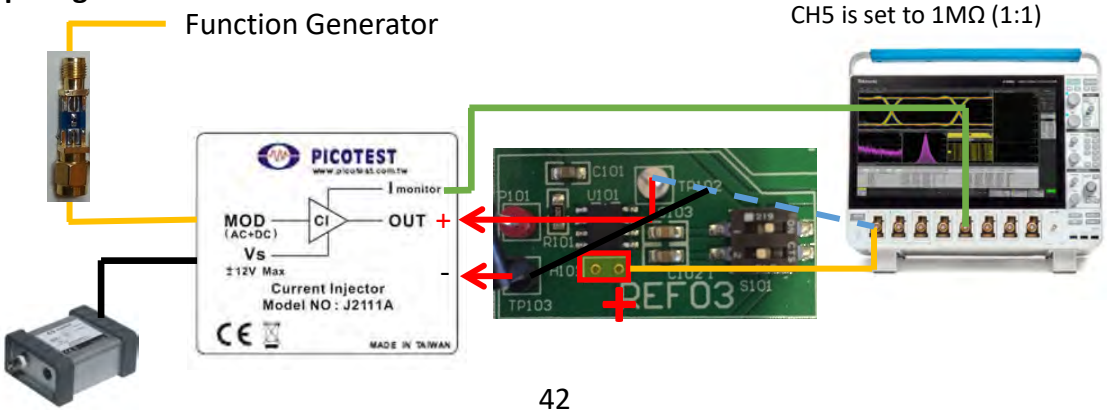
Description:
There are several reasons for step load testing, one of which is that it provides an assessment of the stability of the control loop. A second reason for step load testing is to assess voltage excursions. A step load could also be used to assess the Q of passive filters, such as a ferrite bead and its associated decoupling capacitors, to assess the non-linearity of a circuit with respect to operating load current, to gain insight into the large signal behavior of a circuit, or to determine the susceptibility of other circuits that are connected to the circuit under test. This test measures the step load of a voltage reference.

Instrument	Oscilloscope
Injectors	499Ω resistor, J2111A Current Injector, J2170A High PSRR Adapter
Probe point	TP102, TP103
Probes	1-Port Probe, 10:1 Voltage Probe

Setup file: Open the setup file **volt ref step.tss**
Measurement Steps:
1. Set the switches S101-1 and S101-2 to the first configuration shown above.
2. Setup the function generator. Frequncy of 10kHz, 2.5Vpp, and 2.5V offset.
3. Connect the function generator to a 499Ω resistor.
4. Connect the resistor to the MOD of the J2111A.
5. Connect the Vs of the J2111A to the J2170A.
6. Connect I_monitor of the J2111A to CH5 of the Oscilloscope.
7. Connect the positive and negative OUT of the J2111A to TP102 and TP103, respectively, using banana to mini-grabber cables.
8. Set the bias switch of the J2111A to the OFF (middle) position.
9. Probe H101 to measure the step load response using the 1-port probe.
    - Make sure the Channel settings are correct.
    - CH1 is the output voltage and CH5 (trigger) is the applied load step.
10. Save the waveform and repeat the measurement by setting the switches S101-1 and S101-2 to the second configuration.

Setup Diagram:

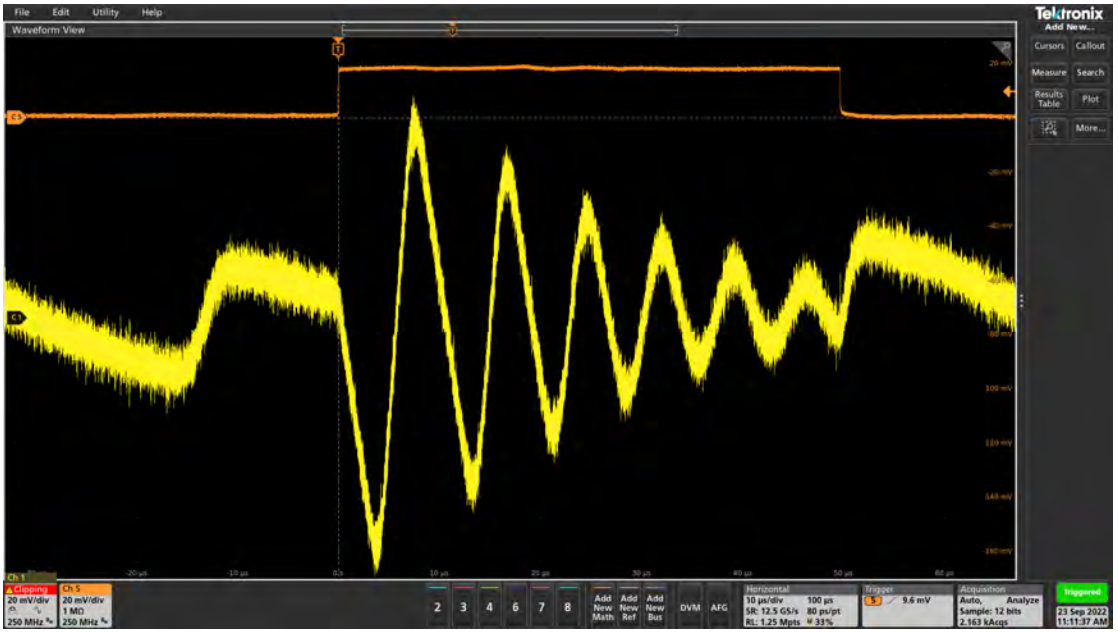
CH1 is set to 1MΩ (1 Port Probe)
CH1 is set to AC (1:1 Probe)
CH5 is set to 1MΩ (1:1)



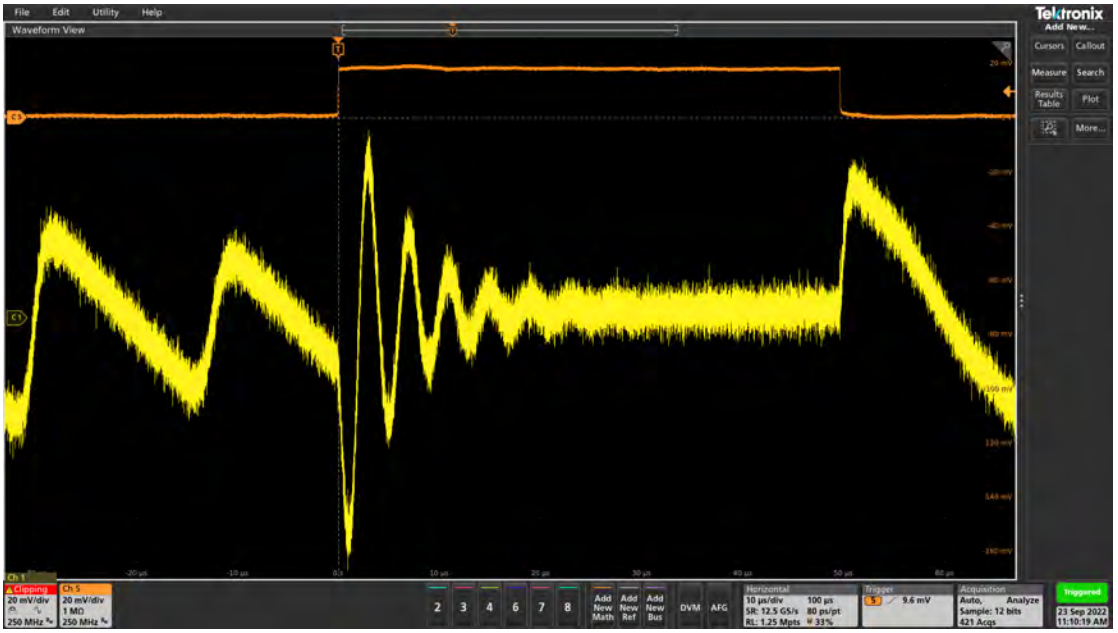
Demo Board Settings:

	First Configuration		Second Configuration	
USB	S101-1	S101-2	S101-1	S101-2
ON	ON	OFF	OFF	ON

Results:



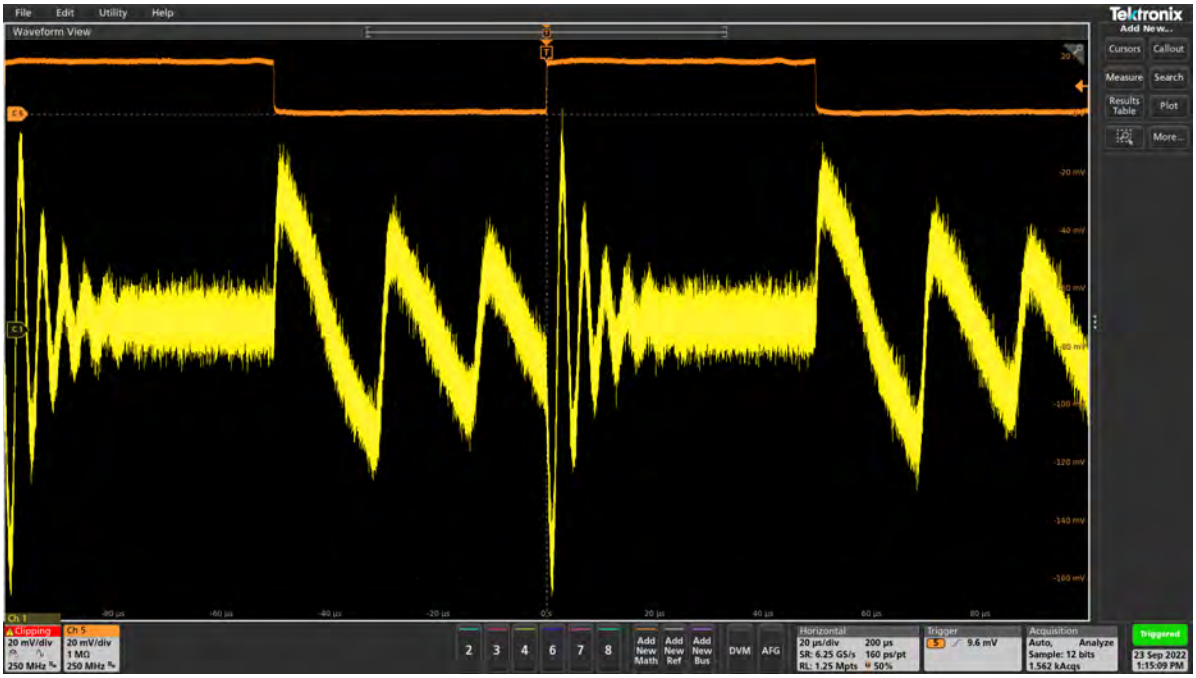
Output of the voltage reference step load with the first configuration.



Output of the voltage reference step load with the second configuration.

Other things to try:

- Connect a voltage probe and observe the step load. Also set both switches to the right.



Using the 1-Port probe to measure the output voltage when both switches are closed.

Using a voltage probe to measure the output voltage when both switches are closed.

Hopefully, you now know how to measure the step load response of a voltage reference. We can also see how different capacitance affects the step load and how it can help reduce the instability of the PDN.

Additional Resources: Power Integrity. Pages 217-232

LDO Regulator Step Load

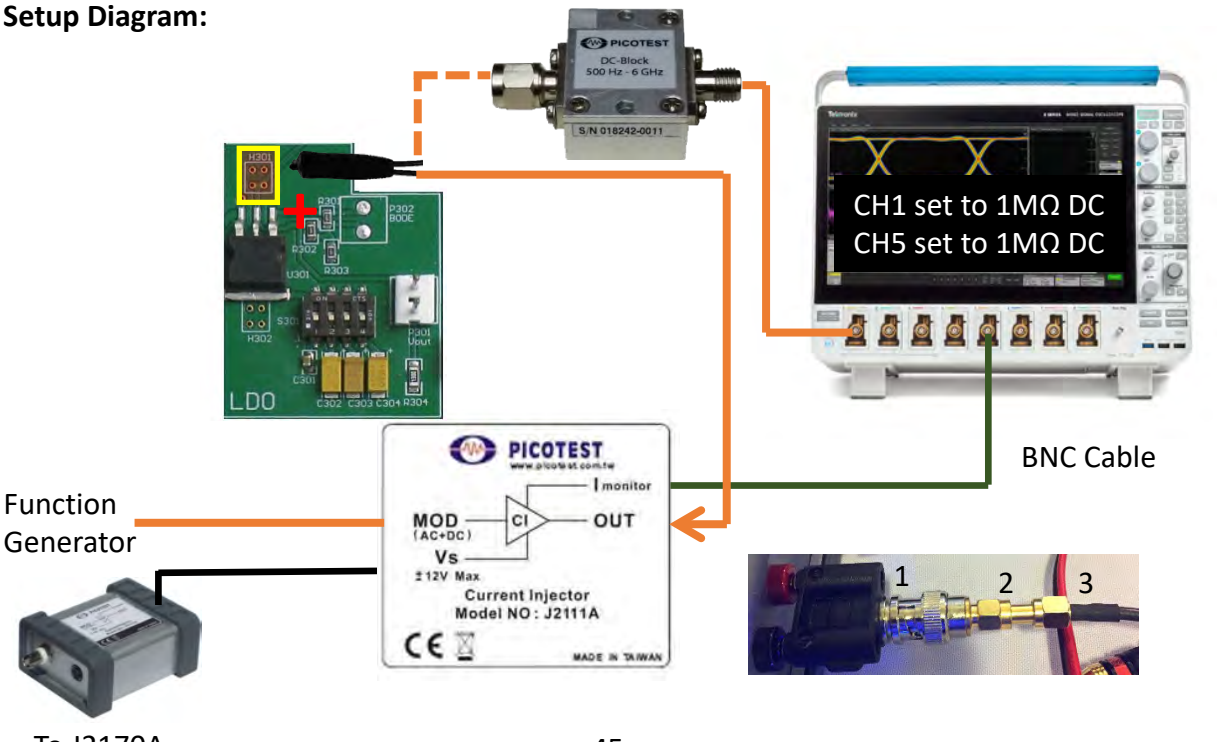
Description:
This test highlights one of the main uses for the 2-Port probe. The ability to both inject and record a signal at the same time. This test measures the step load of an LDO regulator under changing load (stability) conditions. The spectrum of the step load response is also examined.

Instrument	Oscilloscope
Injectors	J2111A Current Injector, J2170A High PSRR Adapter, P2130A DC Blocker,
Probe point	H301
Probes	2 port probe

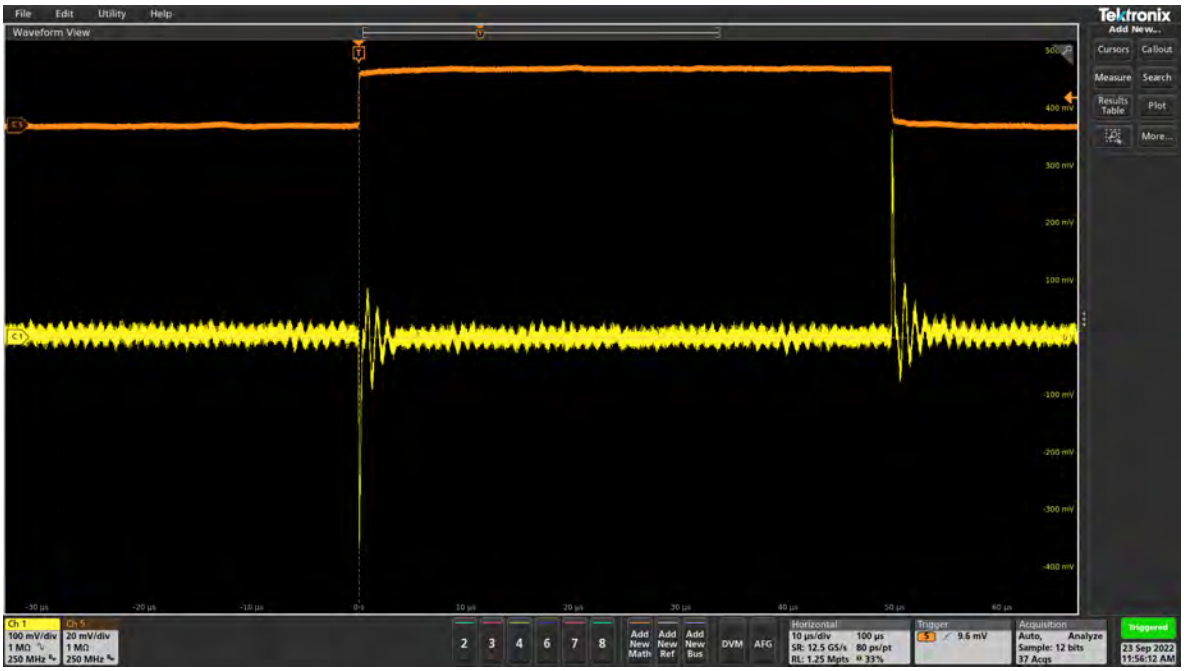
Setup file: Open the setup file **ldo step load.tss**
Measurement Steps:

1. Set the switches of S301 to the configuration shown above.
2. Connect the Function Generator to MOD of the J2111A.
3. Connect the Vs of the J2111A to the J2170A.
4. Connect Imonitor of the J2111A to CH5 of the oscilloscope.
5. Connect one port of the 2-port probe to the OUT of the J2111A.
6. Connect the other port of the 2-port probe to CH1 via the P2130A block.
    - CH1 is the output voltage and CH5 is the applied load step.
7. Probe H301 using the 2-port probe to measure the step load response.

Setup Diagram:



Results:



The step load response is shown on CH1 and the applied load step is shown on CH5. The amount of ringing is related to the stability of the system. The step load response shown above is for the case when only switch S301-1 is ON.

Other things to try:

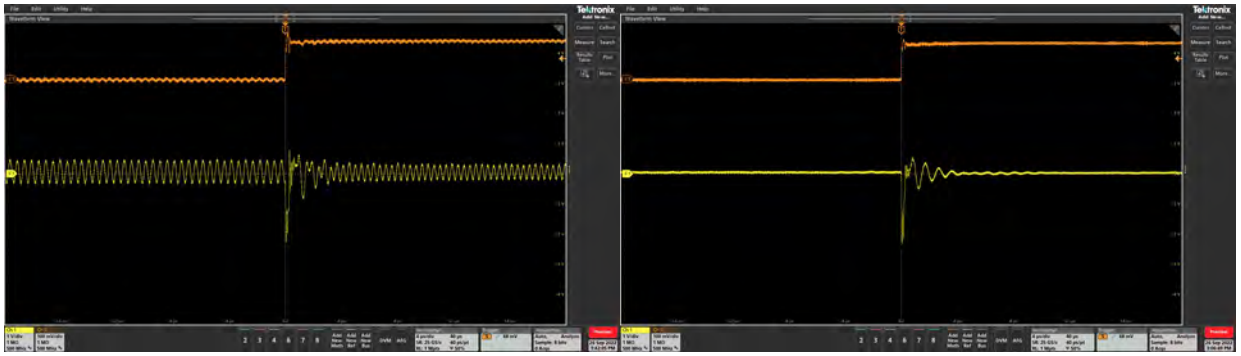
- Try different combinations of S301 switches and repeat the measurement.

S301-1 S301-2

S301-3 S301-4

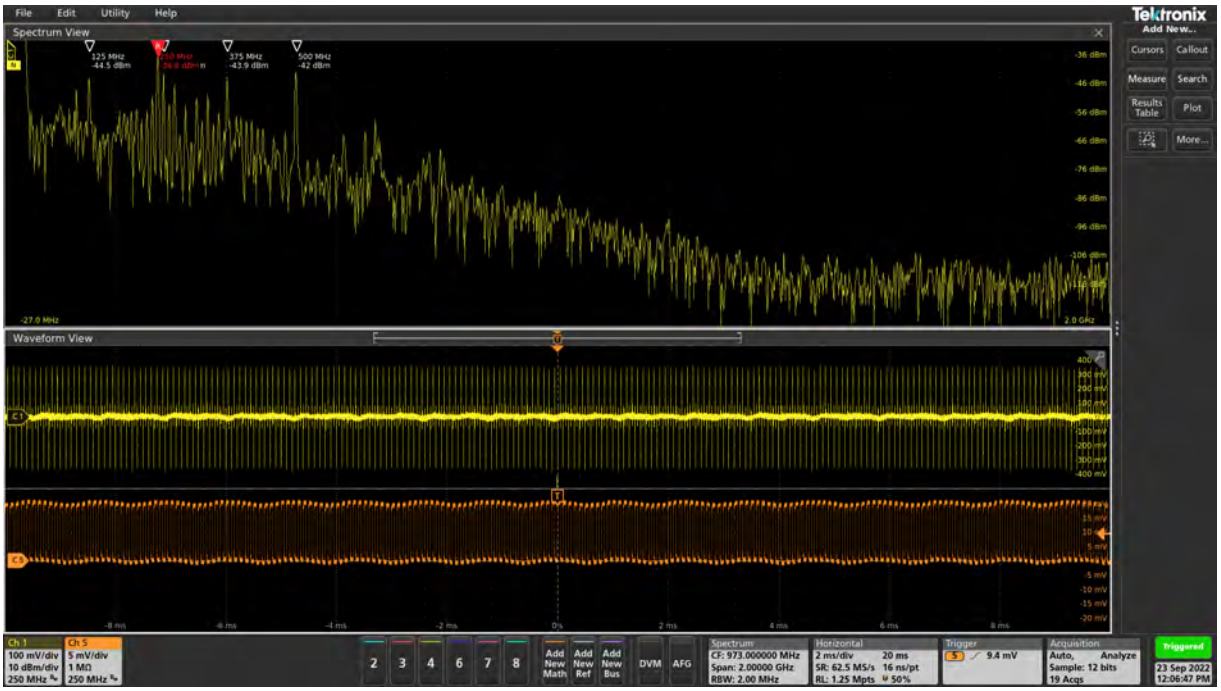
Other things to try:

- Explore the different capacitive loadings by turning ON and OFF switches on S301.



No capacitor measurement is on the left while all the capacitors are active on the right. As you can see the ringing is greatly reduced with the capacitors. Even if just one capacitor is on (look at previous page results), it significantly reduces the ringing and increases the stability of the PDN.

- Open Spectrum view and observe the spectrum for the step load response.



Hopefully, you know how to measure the step of an LDO and how to use the 2-Port probe to measure the step response. The unique thing of the 2-port probe is that it can both measure and inject a signal at the same time. We also explored how different capacitive loading can affect the step load of the LDO.

Additional Resources (Power Integrity, pages 217-232):

Target Impedance

Introduction:
The 2-port measurement is another way to measure the impedance of the DUT. The 2-port measurement is able measure ultra-low impedances, in the μΩ to Ω range. The frequency range of the measurement is limited only by the accuracy of the calibration and the bandwidth of the VNA. The 2-port measurement only requires a thru calibration, which is an even easier calibration than the 1-port measurement. The measurement can also be made at zero volts and biased which means you can measure both an ON state and an OFF state. It can be AC coupled using a DC blocker to eliminate the DC voltage limitations of the measurement. The 2-port is the most accurate low-impedance measurement.

Unfortunately, the DC coupled measurements are limited to 5V because of the power ratings of the 50Ω ports. The 2-port requires additional injectors to combat the DC ground loop that exist. It also requires a multiport probe.

We will be exploring the 2-port measurement and its capabilities. We will learn ways to improve the measurement using series resistors and/or transformers.

We will start off with the most basic 2-Port measurement. **2-Port Shunt Thru Impedance** will allow us to explore ultra low impedances and compare the two ways to break the ground loop using the J2102B and J2113A. We will then learn how to extend the range using the **2-Port Shunt Thru Impedance Extended**. We will also learn how to extract data from components in **Extracting the Capacitor Mount**. Final experiment is how to use 1-Port probes to conduct a 2-Port shunt thru impedance measurement. We will showcase the **Two 1-Port Probe Impedance Measurement** and compare the two methods.

2-Port Shunt Thru Impedance

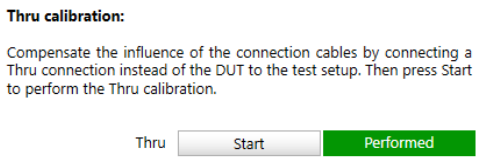
Description:
The two-port shunt thru method allows the measurement of ultra-low (µohms to ohms) impedance values. Limitations introduced due to the resistances of the ground braids of the two cables being in parallel with each other and in series with the DUT can be remedied by using a coaxial 50Ω common mode transformer or by using a semi-floating or differential input. This test measures the impedance of a 1mΩ resistor.

Instrument	Bode 100 VNA
Injectors	J2102B Common Mode Transformer and J2113A Differential Amplifier
Probe point	N/A
Probes	N/A

Setup Files: Open the setup file **1mOhm_shunt.bode3**
Calibration:
1. Connect the OUTPUT of the Bode to CH2 of the VNA using cables and a barrel.
2. Select the "Shunt-Thru" impedance measurement.
3. Perform the THRU (Full Range) calibration.

Measurement Setup:
1. Replace the barrel with the 1mΩ test resistor.
2. Click the Single icon to run a single sweep.
3. Trace 1 displays the impedance of the 1mΩ resistor.

Setup Diagram:



A female barrel is used to short the two cables to together for calibration

BNC to SMA Cable

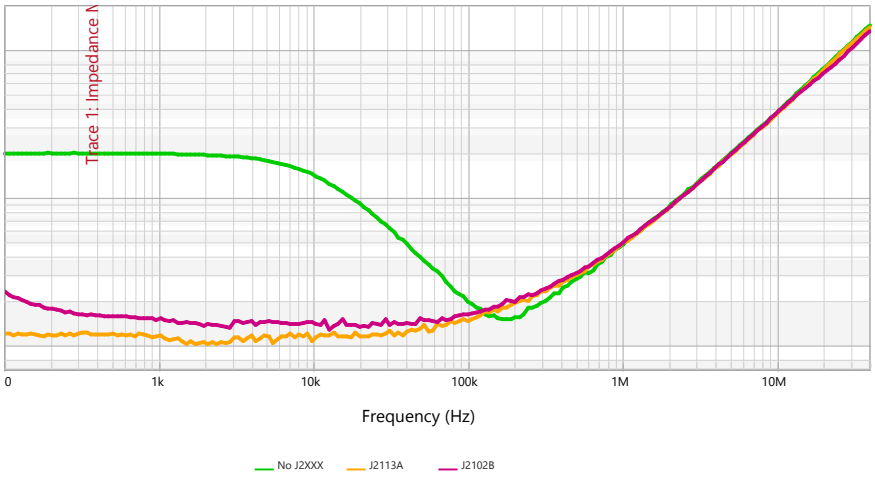
BNC to SMA Cable

1mOhm resistor

Why do you get an open impedance when you put in a shorting barrel?

Because in shunt there is no DUT

Results:



Why do the measurement results change when the J2102B is used?

[We remove some of the ground braid resistances.]

Other things to try:

- Redo the measurement with the J2102B and/or the J2113A.

Transformer Isolator (J2102B)

- Does not go down to DC
- Higher mid-frequency CMRR
- Supports max instrument voltage
- Higher maximum frequency
- Lower noise
- Does not require external power supply
- Lower Price

Solid State Isolator (J2113A)

- Goes down to DC
- Lower mid-frequency CMRR
- 1.8V max input
- Lower maximum frequency
- Higher noise
- Requires external power supply
- Higher price

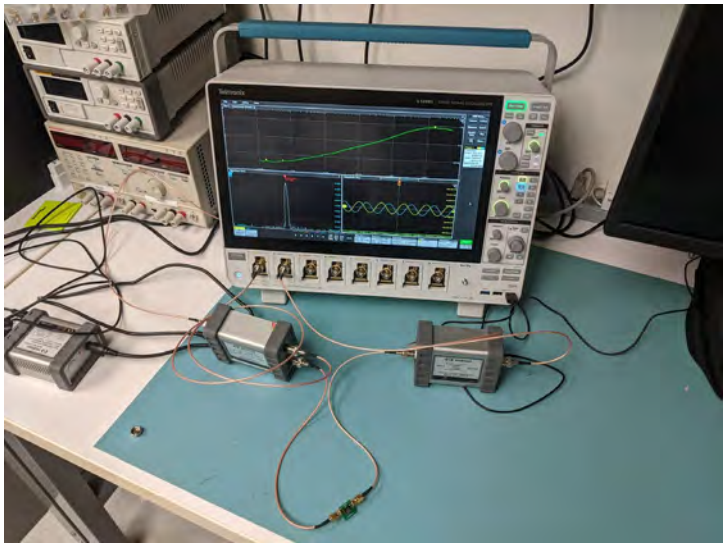
The J2113A is a better choice if you need to measure below 3kHz and below a maximum frequency of 500kHz. Due to the limited CMRR, the J2113A is not recommended below 1mOhm.

Hopefully, you know how to take a 2-Port shunt thru impedance measurement. One can observe that the 2-port can measure small impedances better than the 1-port probe. You also explored different injectors and how that affects the measurement by disturbing the ground loop resistances.

Additional Resources (Power Integrity, pages 123-139):

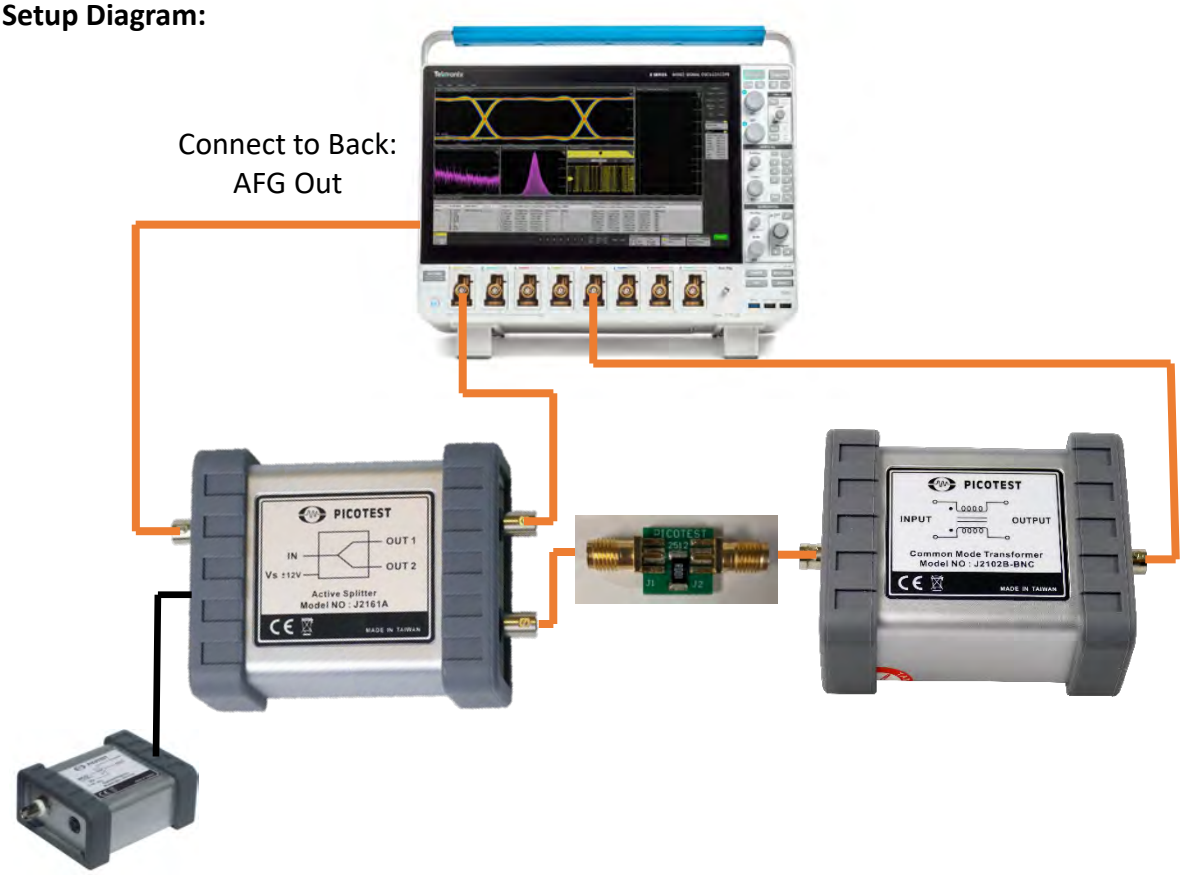
http://electronicdesign.com/boards/how-measure-ultra-low-impedances

Other things to try:
Measure the 2-Port impedance using the Tektronix MS06. The Tektronix scope can be used to measure a 2-port impedance measurement.
Setup Files: Open the setup file **1mohm z.tss** and **ind z.tss**



The setup is very similar to the 2-port shunt thru impedance measurement. It requires a transformer isolator, but it also requires the J2161A Active Splitter to split the internal function generator to go back to the scope and as the input to the DUT.

Setup Diagram:

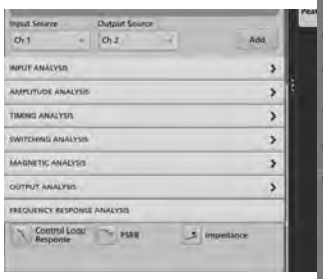


Other things to try:

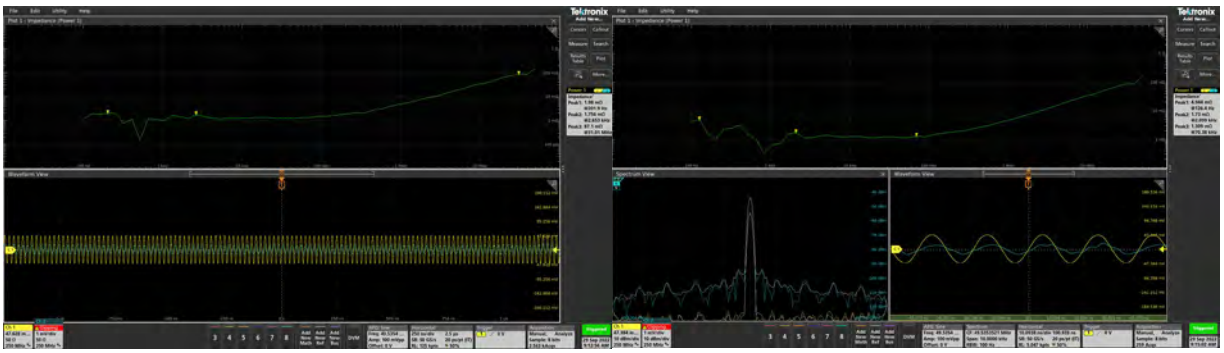
Measure the 2-Port impedance using the Tektronix MS06. The Tektronix scope can be used to measure a 2-port impedance measurement. We measured a 1mΩ resistor to make sure everything is working properly. Then, we measured an inductor's output impedance.

Measurement Steps:

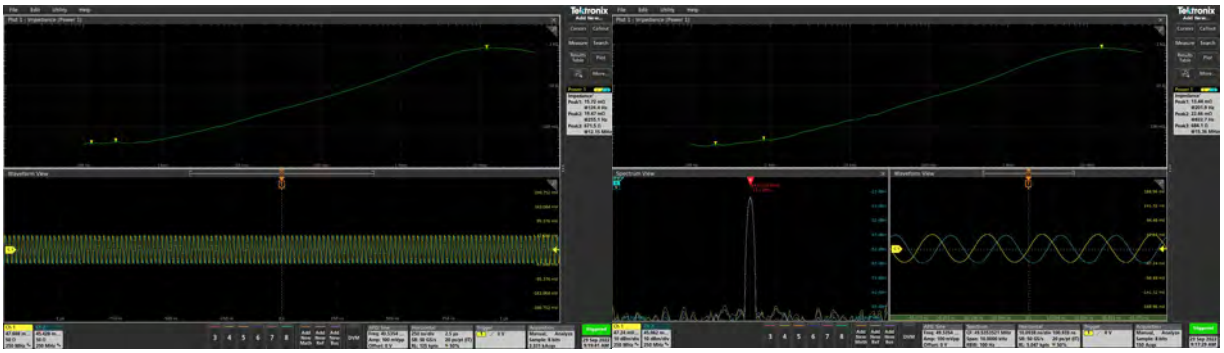
1. Select "Measure" → "Power" → Frequency Response Analysis → Impedance.
2. Set up the AFG by adding AFG at the bottom
3. Double click the "Power 1" measurement and set your desired parameters.
4. Click "Power Preset" and Hit "Run/Stop" to start a measurement.
    - If you want to change resolution bandwidth, click the "Spectrum" window on the bottom and change accordingly.



Results:



1mΩ impedance measurement



1.8nH inductor impedance measurement

There are two output impedance measurements on the MS06. One uses the spectrum view, and one uses the FFT. Both should work but the default is spectrum view and that is fine. You can see that for the 1mΩ measurement, we still get a pretty decent measurement: ~1.039mΩ.

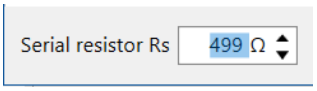
2-Port Shunt Thru Impedance Extended

Description:
This variation of the 2-port shunt thru measurement extends the impedance range that the measurement can support. This extension is useful for measuring impedances that vary widely such as those encountered with opamps, low power voltage references, and linear regulators that span the 1-port and 2-port measurement ranges. The extension process is simple. Here we add a 499Ω resistor to each leg.

Instrument	Bode 100 VNA
Injectors	N/A
Probe point	N/A
Probes	N/A

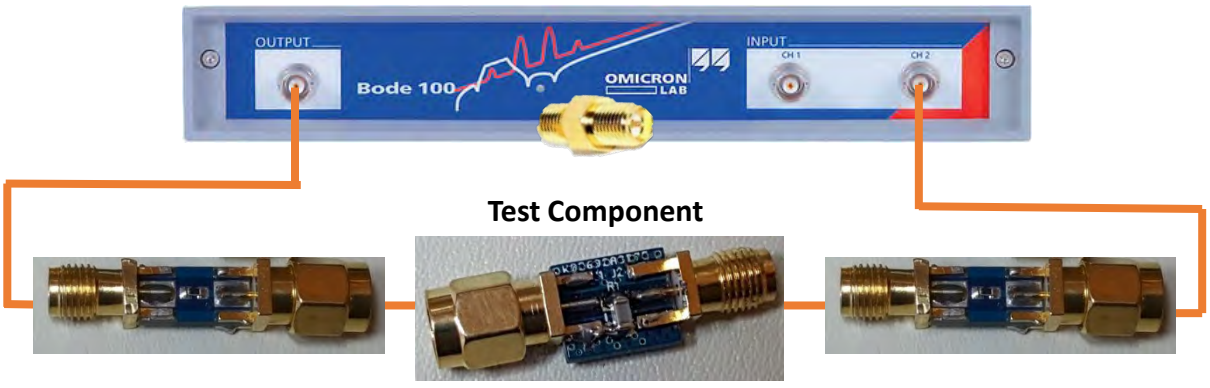
Setup Files: Open the setup file **2-port extended.bode3**
Calibration:
1. Connect Output and CH2 of the Bode 100 to the 499Ω resistors.
2. In place of the test DUT insert a short (female barrel).
3. Select the "Shunt-Thru with series resistance" impedance measurement.
4. In the Full Range Calibration dialog set the Serial resistor Rs to 499 (press Tab or Enter).
5. Perform a (THRU) calibration.

Calibration Note: Keep the 499Ω resistors inline during calibration.



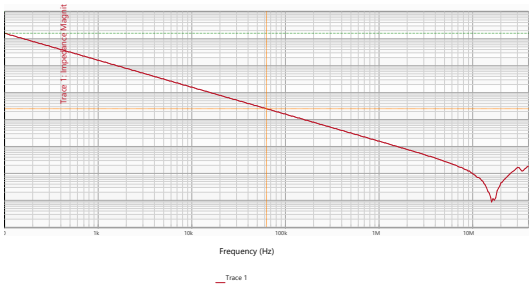
Measurement Setup:
1. Replace the short (female barrel) with the desired test component.
2. Trigger the measurement if needed.
3. Trace 1 displays the impedance.

Setup Diagram:

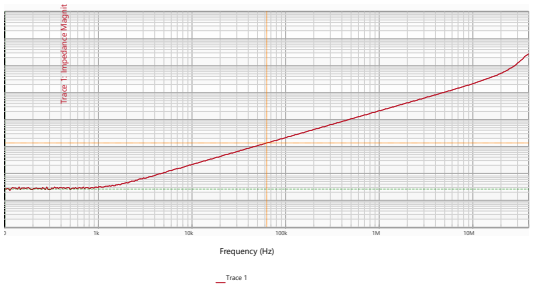


We extend the range by increasing the reference impedance of the VNA. If we can increase the reference impedance from 50Ω to 500Ω, we can increase the measurement range while maintaining the dynamic range. However, this setup lowers the SNR and lowers the signal level. For some measurement, the tradeoff needs to be accounted for.

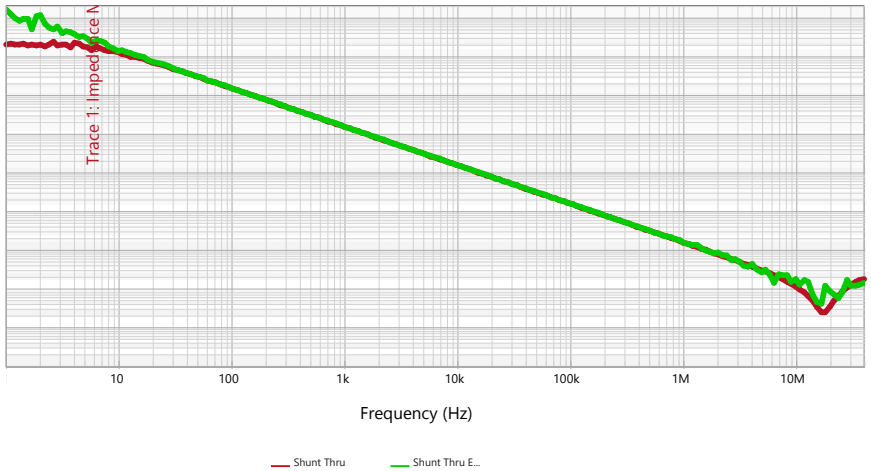
Results:



0.1uF COG Shunt Capacitor



1.8uH Inductor



We can observe the impedance measurement of a capacitor and an inductor. Notice how the capacitors slopes downward like an OPEN impedance measurement and the inductor slopes upward like a SHORT impedance measurement.

The bottom measurement is the result of the extended shunt thru measurement compared with a standard shunt thru measurement.

The extended range measurement shifts the range up in this case so the minimum impedance that can be measured is in the 5-10mΩ range. The benefit is the greatly extended high impedance measurement capability. The green trace were able to measure higher impedances while still maintaining the measurement at 20mΩ. The resolution at resonance is a function of the number of data points.

Hopefully, you now know how to extend the impedance measurement range for the 2-port shunt thru. This is a way to alleviate some of the problems with the 2-port shunt thru measurement. In this way, one can measure a whole range of impedances by putting the appropriate resistor in series with DUT.

Extracting the Capacitor Mount

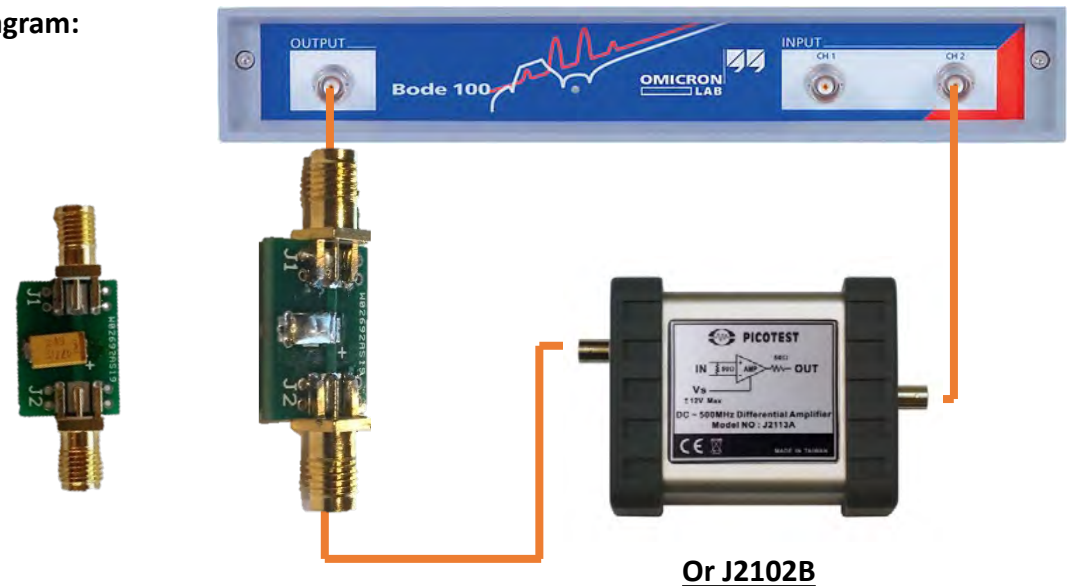
Description:
The capacitor measurement is made up of the capacitor itself and the resistance and inductance of the PCB connections. EM simulators will include the PCB connections, so they need to be removed from the measurement for EM simulation. We need to include the mount for non-EM simulation.

Instrument	Bode 100 VNA
Injectors	J2102B or J2113A Differential Amplifier
Probe point	N/A
Probes	N/A

Setup and Calibration:
1. Connect one side of DUT to the "Output" of the Bode100.
2. Connect the other side to the "Input" of the J2102B or J2113A.
3. Connect the "Output" of the J2102B or J2113A to Ch2 of the Bode100
4. Replace the DUT with a through connection barrel.
5. Select the "Shunt-Thru" impedance measurement.
6. Perform the THRU (Full Range) calibration as you did in the basic Two-Port Shunt Thru measurement.
7. After calibration is finished, put in the capacitor mount board.

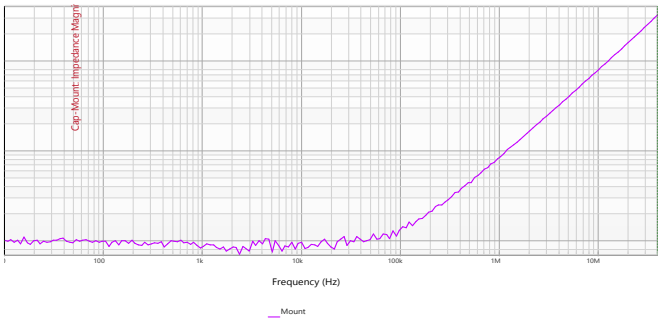
Measurement Setup:
1. Replace the barrel with the Shorted Capacitor Mount Board.
2. Mount the board close to the Output connection.
3. Click the Single icon to run a single sweep.
4. Trace 1 displays the impedance of the shorted mount.
5. Save the Mount trace to memory.

Setup Diagram:

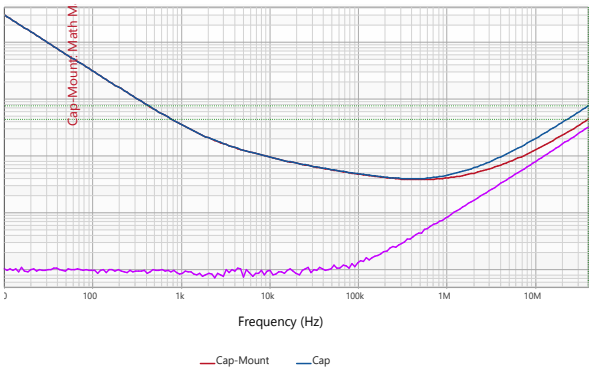


Or J2102B

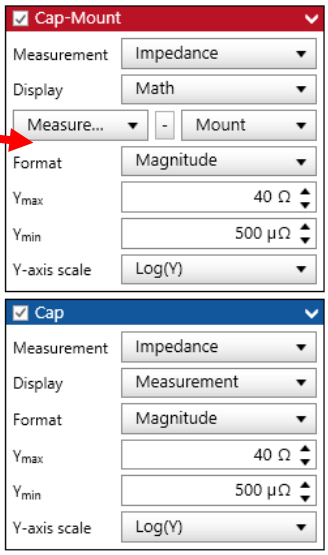
Results:



Expected shorted Mount result with the J2113A. You may note the inductance using cursor 1 with TRACE 2 set to a Format of Ls (@ 40MHz).



Perform the mount subtraction using the Display Math option. The displayed waveform should be setup to be the Measurement minus the saved Mount waveform



The result of the subtraction is the true capacitor measurement for EM simulations.

You can export the data to Touchstone

- Select File -> Export -> Touchstone Export
- Network Parameter: Select “Z” (1-Port)
- Select Network Data -> Save as…
- View the file with a text editor

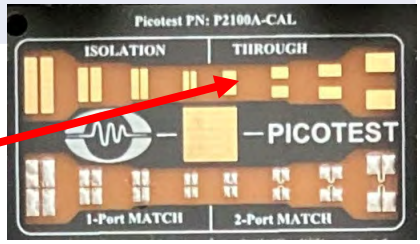
If you need these boards to make the measurement, check out the DTBK01 Decoupling Test Board Kit. These boards and measurements are used for acquiring accurate and high-fidelity data for model support. Especially components of parts that have no standard; if the vendor de-embed the mount.

Hopefully, you know how to extract the PCB board and trace measurements. You should also know more functions in the Bode100 software and how to get a true measurement for components for EM simulations.

Two 1-Port Probe Impedance Measurement

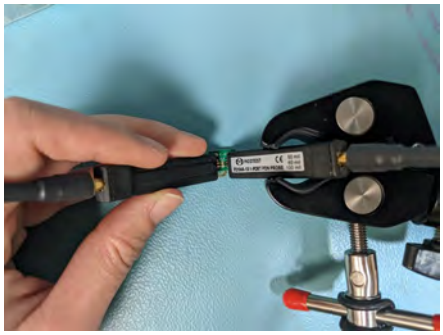
Description:
We can perform a shunt thru impedance measurement using two 1-port probes. One probe will act as one side of the shunt thru while the other probe will act as the other side. We will compare the two 1-port probes' measurement to the shunt thru impedance measurement we performed earlier.

Instrument	Bode 100 VNA
Injectors	N/A
Probe point	N/A
Probes	P2104A 1-port probe

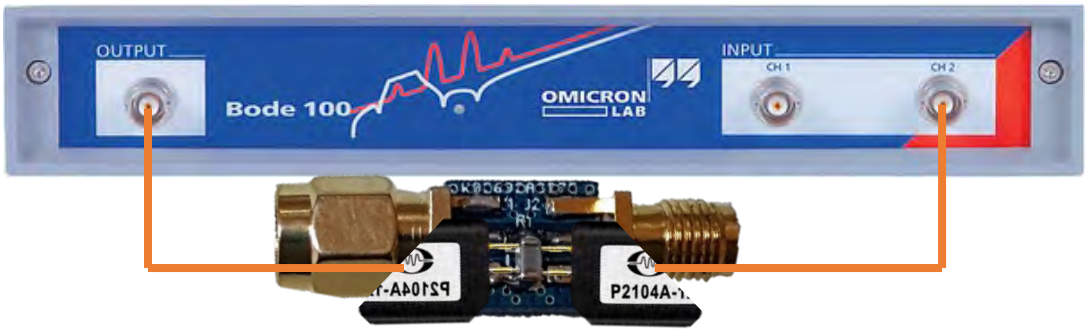


Setup Files: Open the setup file **two_1port.bode**.
Calibration:
1. Connect one probe to the output of the Bode100.
2. Connect the other probe to the Ch2 of the Bode100.
3. Select the "Shunt-Thru" impedance measurement.
4. Use the THROUGH of the calibration board and perform a THRU calibration.

Measurement Setup:
1. Find the 0603 ceramic capacitor.
2. Conduct a 1-Port probe measurement on the cap.
3. Conduct a 2-Port Shunt Thru measurement on the cap.
4. Setup the two 1-Port probes in the diagram.
5. Place one 1-Port probe on the right side.
6. Place one 1-Port probe on the left side.
7. Conduct a SHUNT-THRU measurement.

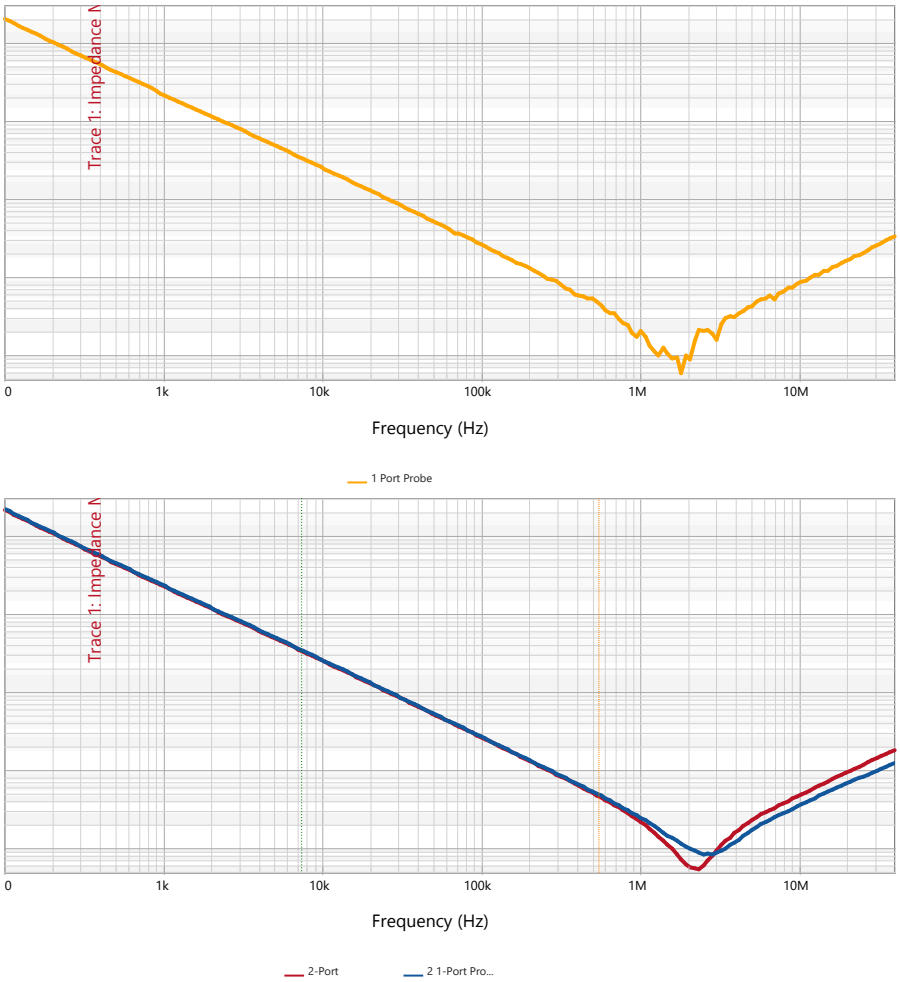


Setup Diagram:



You will need to use a probe holder or may need some help to conduct this measurement. It is also difficult to get the 1-Port probe's pins across the component. Be careful and take your time. Try to get all four pins correctly placed before saving a measurement.

Results:



Here we can see the differences on all the methods we have learned so far. The top graph shows the output impedance with a 1-port probe. See the noisy signal at the ESR. The blue trace is the two 1-port probes measurement. This is a new measurement. See how the signal is cleaner and smoother. Lastly, the red trace is the 2-Port shunt thru measurement. This gave us the best result as it reached the lowest ESR. We can see the differences in all three methods.

For the new measurement method of two 1-Port probe, the angle between the two probes is crucial. When you calibrate the setup, make sure you try to maintain the same angle between the probes for the measurement as you did with the calibration. A different angle changes the inductance and coupling of the probes, which can affect your measurement.

Hopefully, you know three methods for measuring the output impedance. The 1-Port probe is simple to use but does not work well at small impedances. The two 1-Port probes acting as a 2-port shunt thru is better but needs more equipment to make the measurement and is more varied based on the angle between the probes. Lastly, the 2-port shun thru method is relatively simple and can measure small impedances very well.

2-Port Probe Output Impedance

Description:
This test measures the output impedance and stability of an LDO using a 2-port probe and a common mode transformer. The 2-port probe has two leads at the tip (joined with a special pointed clip) and a common ground port. While the connection of the tip and ground wire to the board may take some getting used to, this "browser" class probe is very useful in making multiple measurements in tight places without the need to recalibrate. A measurement of the VRTS1.5 board demonstrates this.

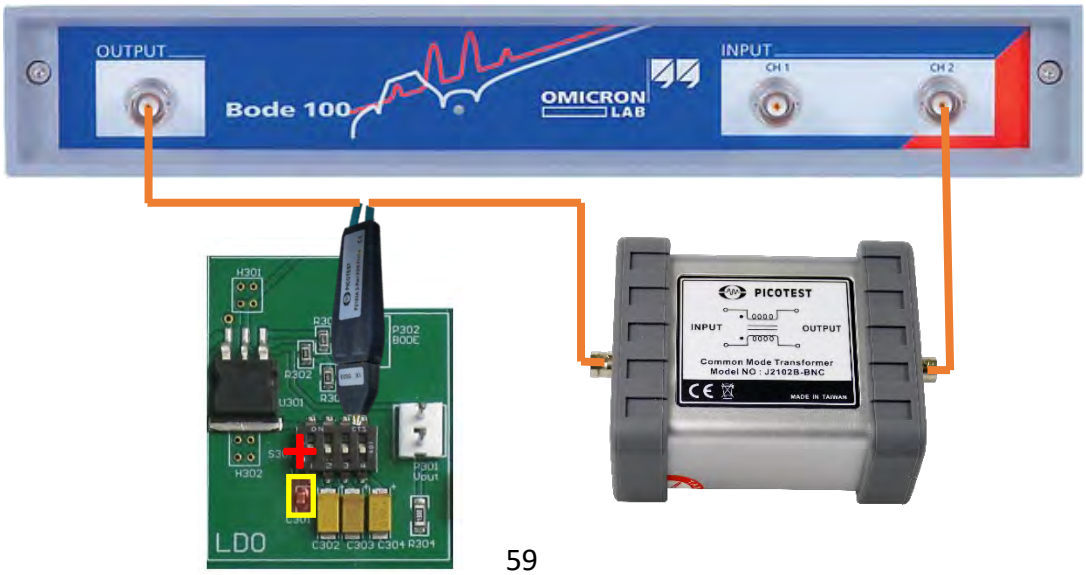
Instrument	Bode 100 VNA
Injectors	J2102B Common Mode Transformer
Probe point	C301
Probes	P2102B 2-port probe (0805 Header)

Demo Board Settings:

SEL1	USB	S301-1	S301-2	S301-3	S301-4
RIGHT	ON	ON	OFF	OFF	OFF

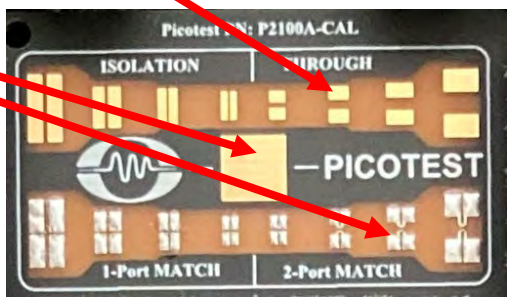
Setup File: Open the setup file **ldo_z.bode3**
Setup:
1. Select the "Shunt-Thru" impedance measurement.
2. Connect one side of the 2-port probe to the "Output" of the Bode100.
3. Connect the other side to the "Input" of the J2102A.
4. Connect the "Output" of the J2012A to "Ch2" of the Bode100.
5. Select and attach the appropriate header for the 2-port probe. For this experiment, it will be 1206 header.

Setup Diagram:



Calibration:

1. Once everything is connected and setup, run a SOL calibration for the 2-port probe
2. Click “Full-range” or “User-range”.
3. The “Open” calibration will be a “Through” measurement.
4. The “Short” is the center pad.
5. The “Load” is the 2-port match measurement.

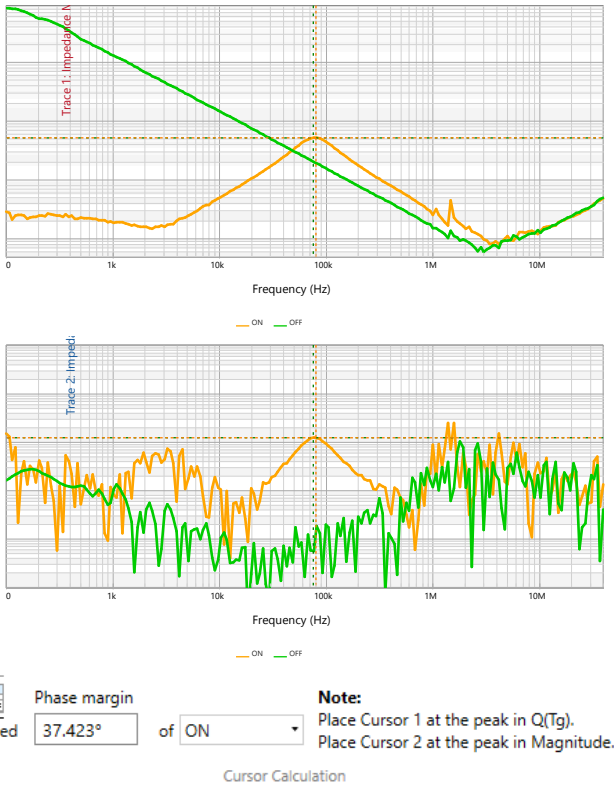


Make sure to test your calibration with a known value of similar magnitude before measuring the capacitor. We usually measure a resistor of known value and verify that the output impedance is a flat line at that known value.

Measurement Steps:

1. Use a DMM to determine the positive side of the capacitor.
2. Put the 2-port probe’s pins around C301.
3. Make the positive end of the probe goes with the positive end of the capacitor.
4. Take an OFF-state measurement and an ON-state measurement.
5. Record the measurements to Memory.

Results:

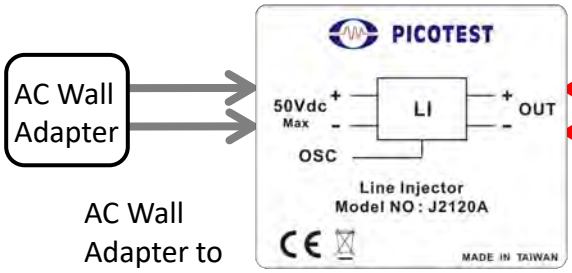


Notice how the ON state (Orange) is different than the OFF state (Green). It is shifted to the right. The series resonance also shifted from ~3MHz to ~4MHz. This is because the ON State has a different DC bias than the OFF state. The DC bias will affect the capacitance and thus give a different output impedance. This can be fixed by adding more capacitance. Another way to fix it, is by adding a pullup resistor to bias the capacitors in the OFF state. Remember, the pullup needs to be bigger than the max impedance so that the measurement is not affected.

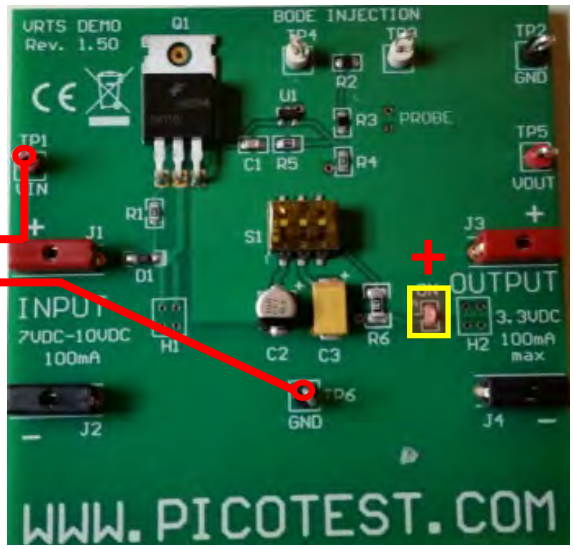
Other things to Try:

- Setup the VRTS1P5 board.

Setup Diagram:

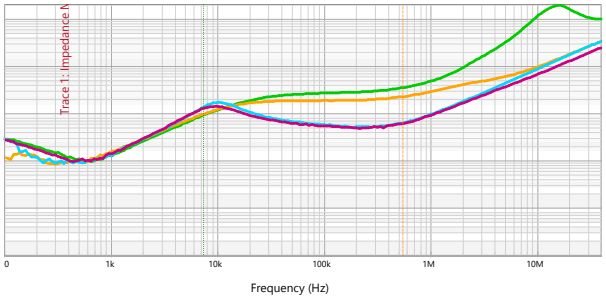


AC Wall Adapter to Banana Plug

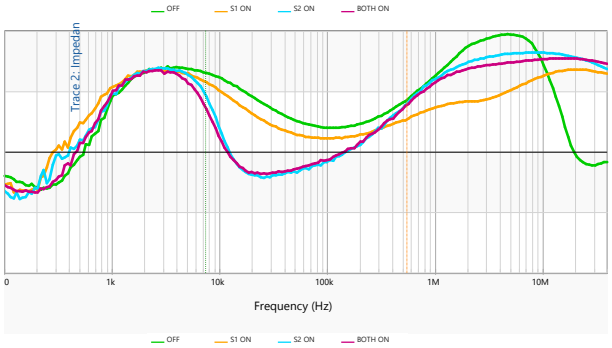


Measurement Steps:

1. Power on the VRTS1P5 board.
2. Set switch S1-1 and S1-2 to the OFF position
3. Place the probe across the LED with the Positive side towards the ON side.
4. Take a measurement.
5. Repeat measurement
    - S1-1 ON and S1-2 OFF
    - S1-1 OFF and S1-2 ON
    - S1-1 ON and S1-2 ON



Output impedance and group delay (Q) of the VRTS1P5 regulator for various load capacitor configurations.

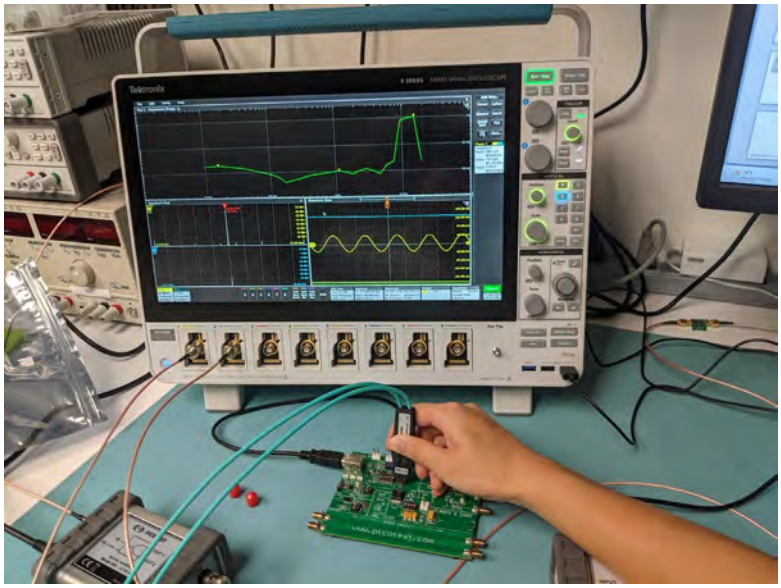


Determining where to probe is difficult. Ideally, we want to probe at the regulating resistors. This is where there will be the least loss of impedance because it is at the source. If we want to choose a new probe point, we must make sure the impedance difference is insignificant to the measurement. If this is the case for everywhere on the board, we can theoretically probe at any point on the board.

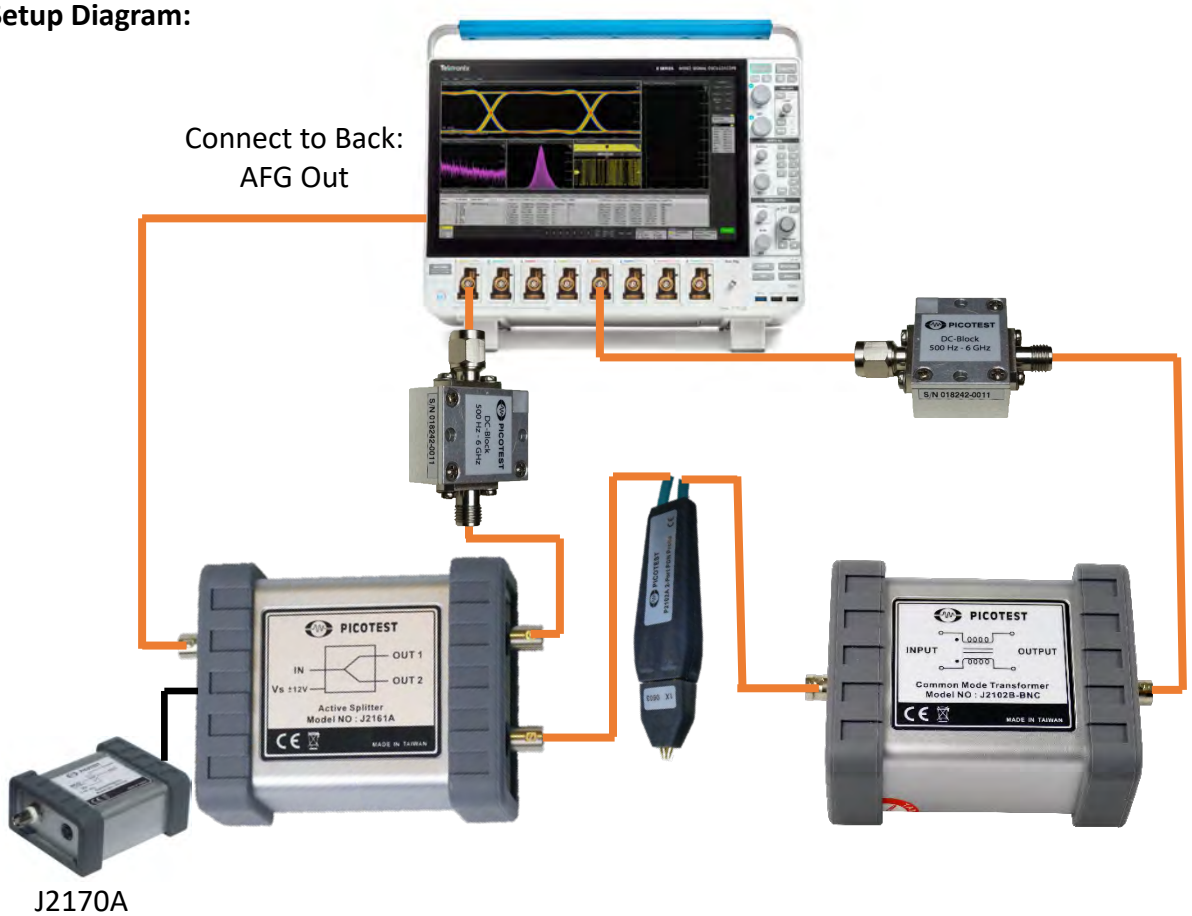
Hopefully, you learned how to calibrate and use a 2-port probe. The 2-port probe calibration is more nuanced, but it can measure much lower impedances with the 2-port probe. Remember to break the ground loops with an injector to have the most accurate results.

Other things to Try:

- Use the MS06 to measure the output impedance using the 2-Port probe.

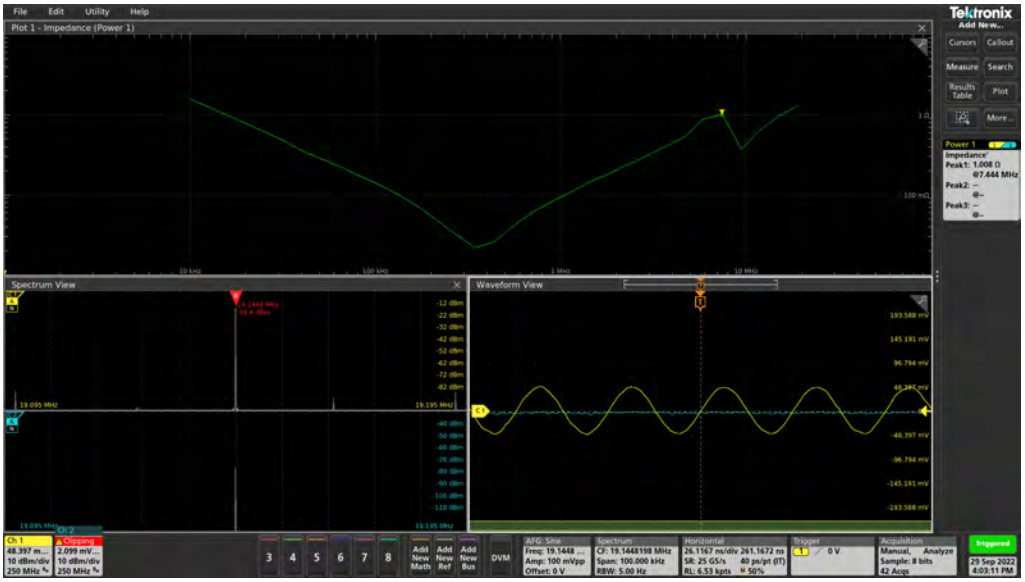


Setup Diagram:

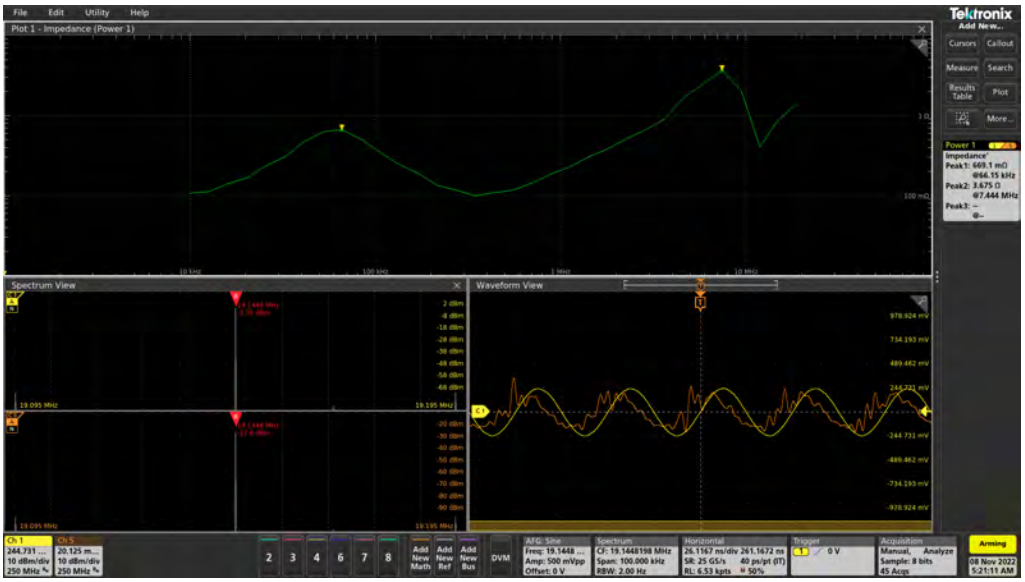


Other things to Try:

- Use the MS06 to measure the output impedance using the 2-Port probe.



The OFF measurement



The ON Measurement

The OFF measurement was like the Bode100. The ON measurement was difficult. The ON measurement had overvoltage on the channel which led to a difficult measurement.

Setup File: Open the setup file **ldo on.tss** and **ldo off.tss**

Design for Flat Impedance

Introduction:
Now that we can measure the impedance and see how it changes across frequency, we can start thinking of ways to design for desired qualities, like a flat impedance. A flat impedance is the most stable. We will be examining factors that affect the output impedance like capacitive loading and decoupling capacitors.

The goal is to create a flat impedance. This can be done by adding capacitors that will offset the inductive nature of components or offset the abnormalities of the printed circuit board (PCB).

Teeter-Totter Effect

Description:
The Teeter-Totter effect refers to the phenomenon observed as a regulator's output impedance changes. When the impedance at the regulator is reduced, the resonant peak at the other end of the trace increases. This effect demonstrates why it's important to match the impedances of the regulator, planes, and load. The impact of impedance on Clock Jitter is also explored.

Instrument	Bode 100, Oscilloscope (Optional)
Injectors	P2130A, Picotest Harmonic Comb (Optional)
Probe point	H401
Probes	1 port probe

Demo Board Settings:

				First Configuration (100uF)				Second Config. (2.2uF)		Third Config. (15uF)	
S401	S402	USB	SEL	S301-1	S301-2	S301-3	S301-4	S301-2	S301-3	S301-3	S301-4
OFF	OFF	**OFF**	Right	OFF	ON	OFF	OFF	OFF	ON	OFF	ON

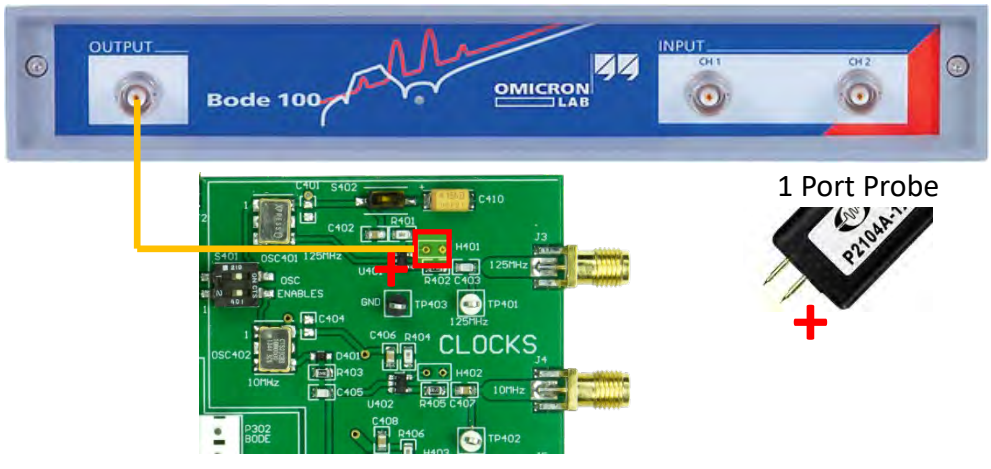
Setup file: Open the setup file **teeter totter OFF.bode3**
Calibration:

1. Connect the 1 port probe to the output of the VNA.
2. Select the "One-Port" impedance measurement.
3. Perform an OPEN-SHORT-LOAD calibration.

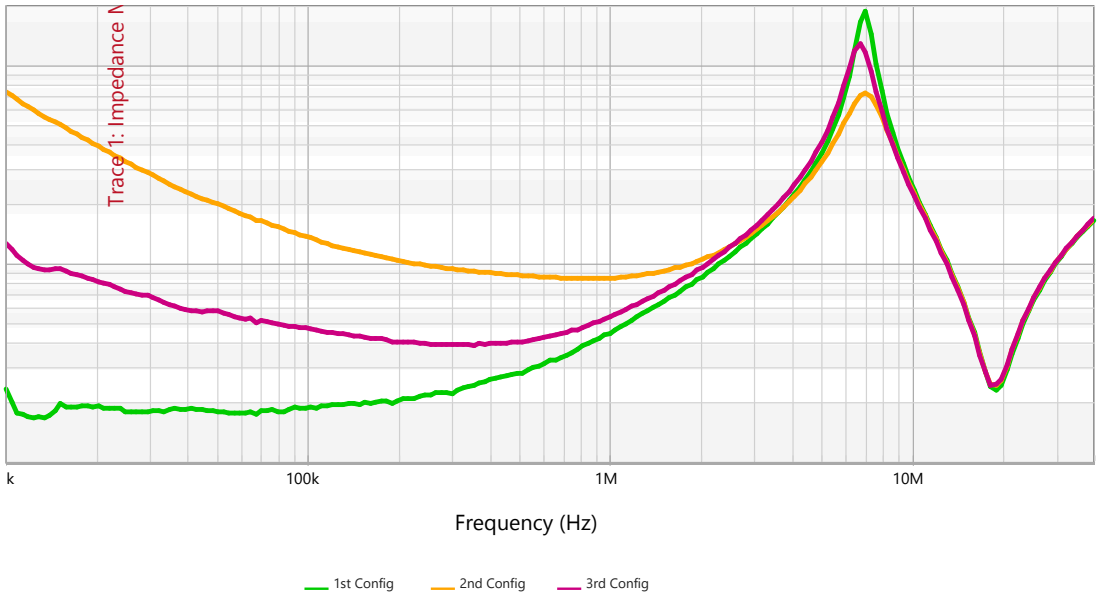
Measurement Steps:

1. Measure the impedance at H401 using the 1-port probe.
2. Save the trace to memory.
3. Repeat the measurement again for the second configuration.
4. Repeat the measurement again for the third configuration.

Setup Diagram:



Results:



The output impedance at H401 is shown above for different capacitor ESR values. As the impedance of the regulator is reduced the resonance peak increases. The highest ESR which is the Orange trance has the lowest peak. The valley is the decoupling cap series resonance.

Hopefully, you know how the different output impedance can affect the measurement. This should reinforce the desire to have matched impedances between the regulator, PCB planes, and loads.

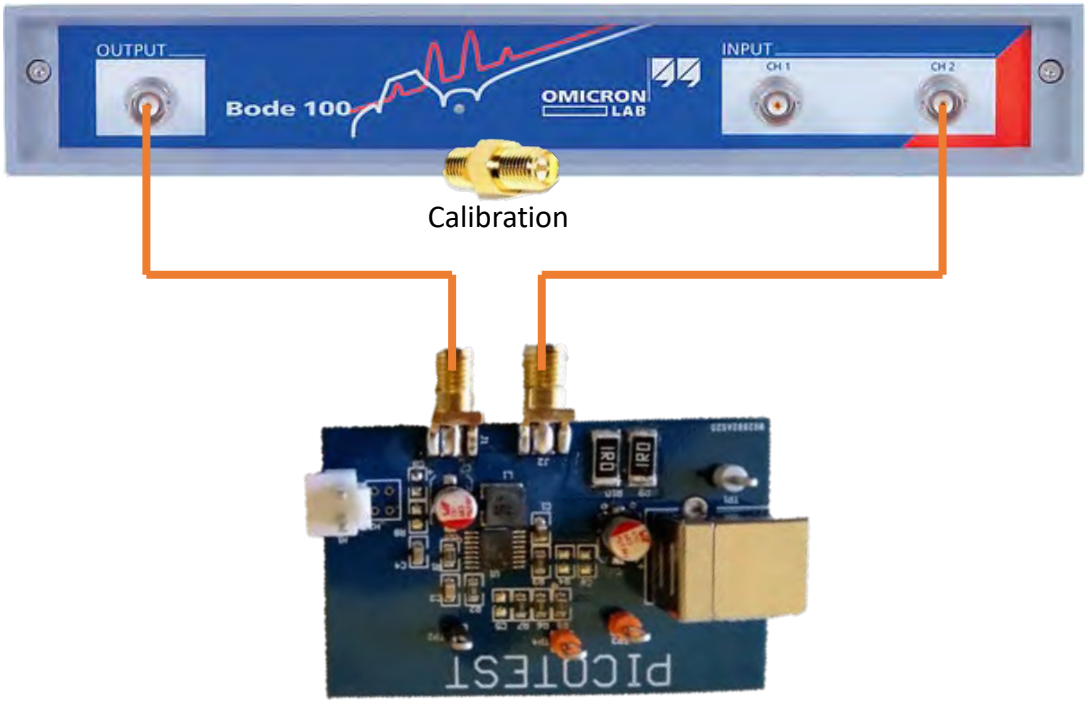
LM20143 Flat Impedance Test

Description:
The circuit is an integrated point of load synchronous buck regulator with a 5V input and a 1.2V/2.5A output. The device uses emulated current mode control, making it simple to create a flat impedance output. Easily accessible 0805 chip size components make it easy to customize or experiment with different component values. This is a fully self-contained demo board using USB input power and an on-board resistive load. Provisions are included for a Bode plot measurement, with the injection resistor, R5. SMA output connectors are also included to simplify connections for many measurements including the 2-port output impedance measurement we are performing here.

Instrument	Bode 100 VNA
Injectors	N/A
Probe point	LM20143 Board Connectors
Probes	N/A

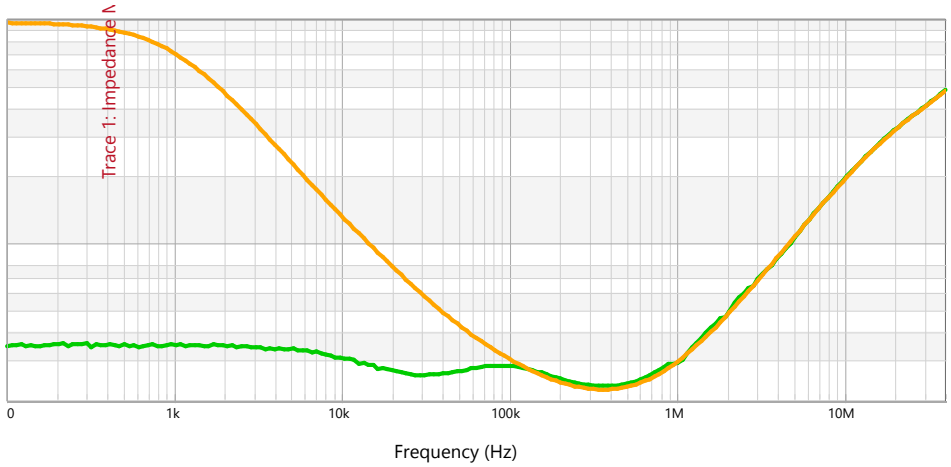
Setup Files: Open the setup file **lm20143_z.bode3**.
Calibration:
1. Select a “Shunt-Thru” measurement.
2. Connect one cable to the Output of the Bode100.
3. Connect another cable to Ch2 of the Bode100.
4. Take a short (female barrel) and perform a THRU calibration.

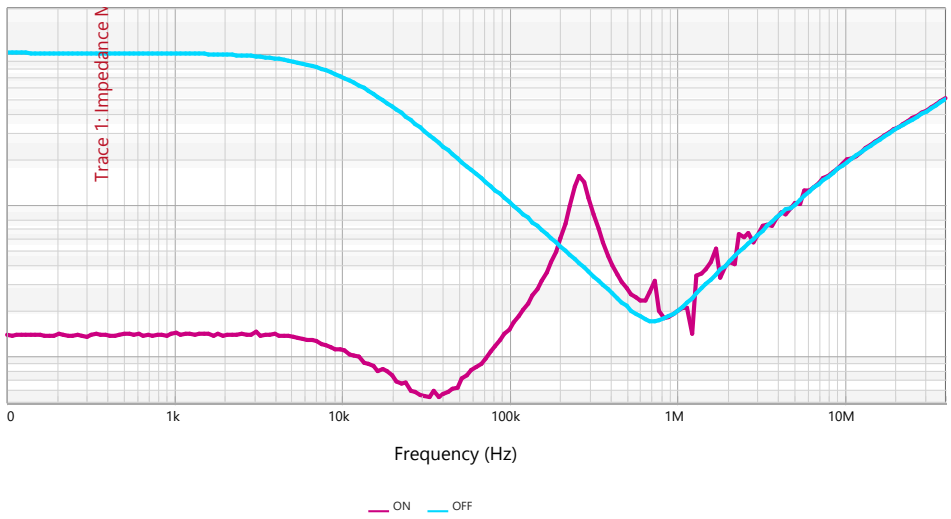
Setup Diagram:



Measurement Steps:

1. Replace the short with the board measurement ports.
2. Record a measurement.





The first measurement shows the ON and OFF state of the LM20143 board. Notice the flat impedance in the ON state.

The VRM ultimately connects to the printed circuit board planes, which are generally inductive. The inductance needs to be absorbed by decoupling capacitors at the load in order to maintain the flat desired impedance. This is accomplished by proper selection and placement of the decoupling capacitors to match the circuit board planes.

The second measurement is the same board with more capacitor or decoupling. Notice how the impedance is not flat anymore. This means that the board is not matched.

Hopefully, you learned about flat impedances and how to measure it. You should also know about how decoupling can help with the inductance in the board but too much can cause a un-flat impedance.

Advanced Tests

Introduction:
We can measure much more than just impedance. Even though impedance can tell us many things, we can use the probes and Bode100 to measure the power supply rejection ratio (PSRR) and the bode plot of the power delivery network (PDN). We can also observe how the PDN is affected by step loads. The probes are versatile tools that can be used to measure and observe many crucial results of the PDN.

We will be using injection transformers to help us measure the Bode plot. A good injection transformer has high flux capacity, very good coupling, adequate isolation voltage and sufficient permeability to allow the low frequency injection. This is useful to get a full range of frequency when trying to measure the Bode plot.

POL Bode Plot

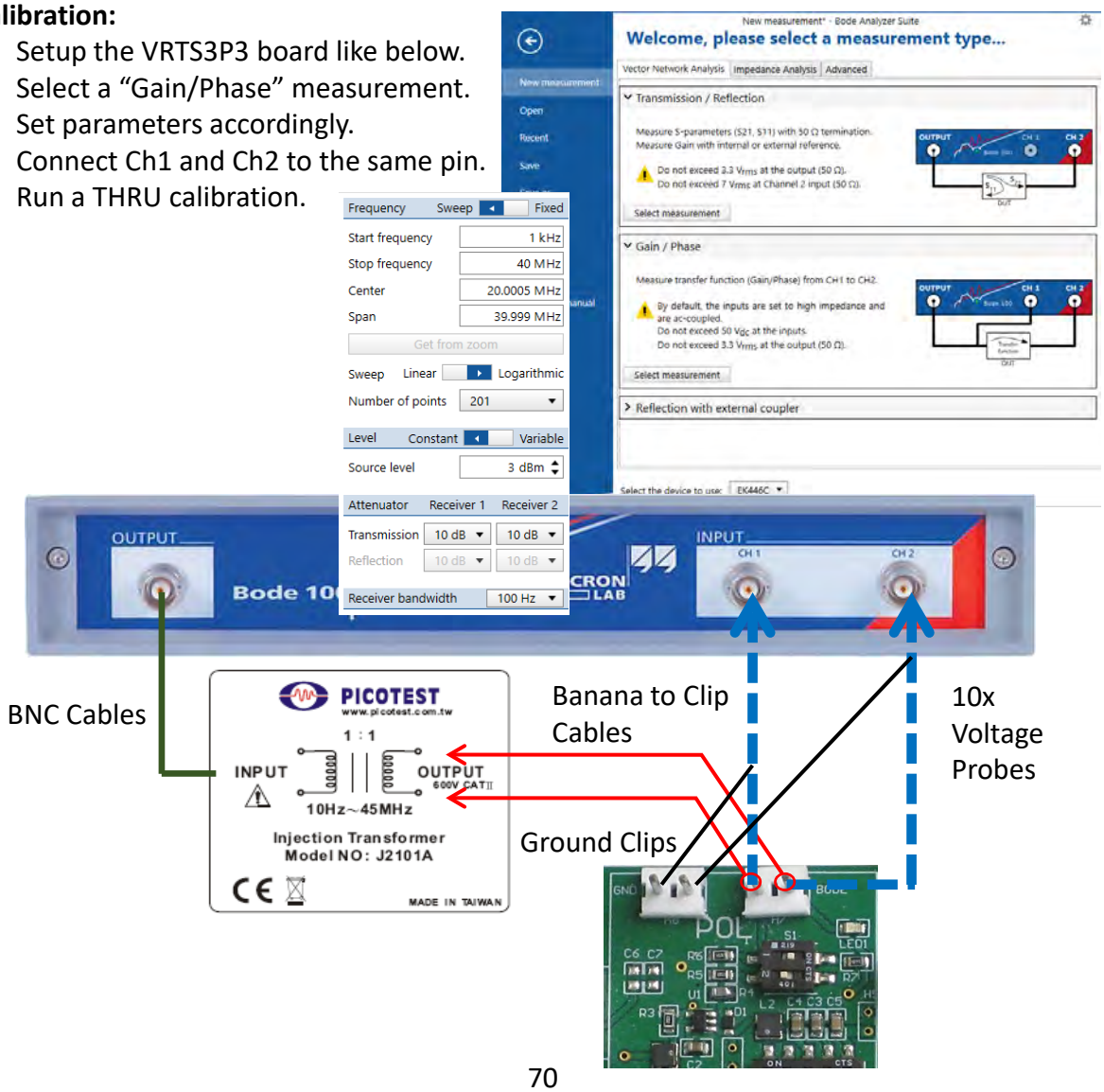
Description:
Control loop stability is traditionally determined from an open loop Bode plot in the frequency domain. Phase margin (phase at 0dB gain) and gain margin (gain at 0° phase) are the two stability assessments. Though systems don't always provide Bode plot access. This test establishes a baseline for comparison with the non-invasive stability assessment.

Instrument	Bode 100 VNA
Injectors	J2101A (or J2100A) Injection Transformer
Probe points	H6 (GND), H7(BODE)
Probes	10:1 voltage probes (2)

Setup file: Open the setup file **pol_bode.bode3.**

Calibration:

1. Setup the VRTS3P3 board like below.
2. Select a "Gain/Phase" measurement.
3. Set parameters accordingly.
4. Connect Ch1 and Ch2 to the same pin.
5. Run a THRU calibration.



Setup file: Open the setup file **pol_bode.bode3.**

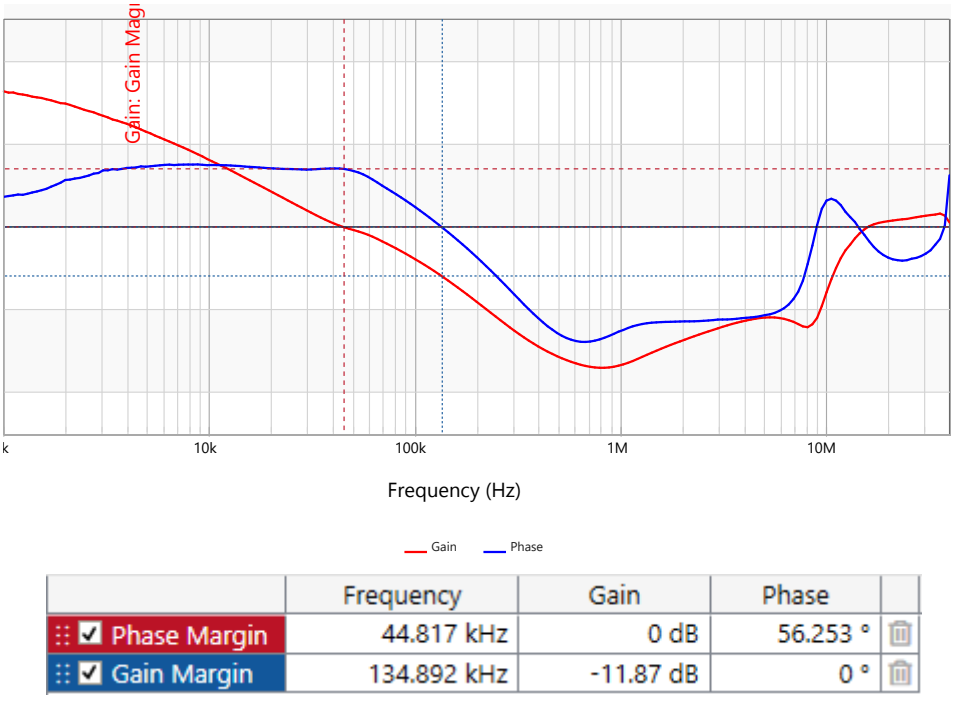
Measurement Steps:

1. Make sure you are setup correctly and verified your calibration.
2. Set the board settings accordingly.
3. Connect the CH1 and CH2 voltage probe to the left and right pins of H7 (move one of the probes to the other pin), respectively.
4. The ground clips remain on H6.
5. Trace 1 will display the gain curve of the POL Bode plot. Trace 2 will display the phase curve. Click the measurement icon.
    - If the Bode plot is upside down, then the connection polarities are not correct. You can split the graph into two separate graphs by using the One axis per chart function in the View menu.
6. Set the cursor to 0dB and record the phase margin value.

<u>Note: Your plot may have a different gain response due to differences in various VRTS3 boards.</u>

Demo Board Settings:

S2-1	S2-2	S2-3	S2-4	S2-5	SEL1	USB	S1-1	S1-2	S401-1	S401-2
OFF	OFF	OFF	OFF	OFF	LEFT	ON	ON	OFF	OFF	OFF

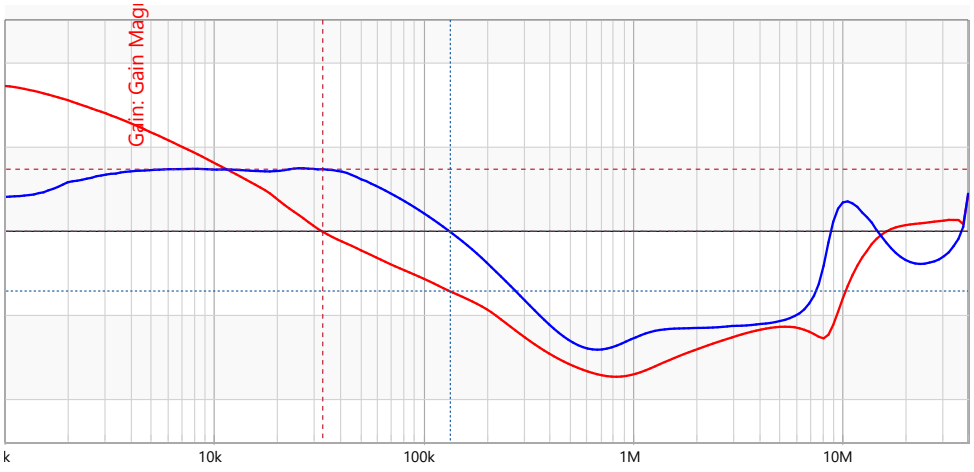


	Frequency	Gain	Phase	
Phase Margin	44.817 kHz	0 dB	56.253 °	
Gain Margin	134.892 kHz	-11.87 dB	0 °	

The recorded measurement is the bode plot of the POL. Through the bode plot, we can find the phase margin by seeing the phase at 0dB. Compare the phase margin to the phase margin we derived using the cursors (POL Output Impedance).

Other Things to Try:

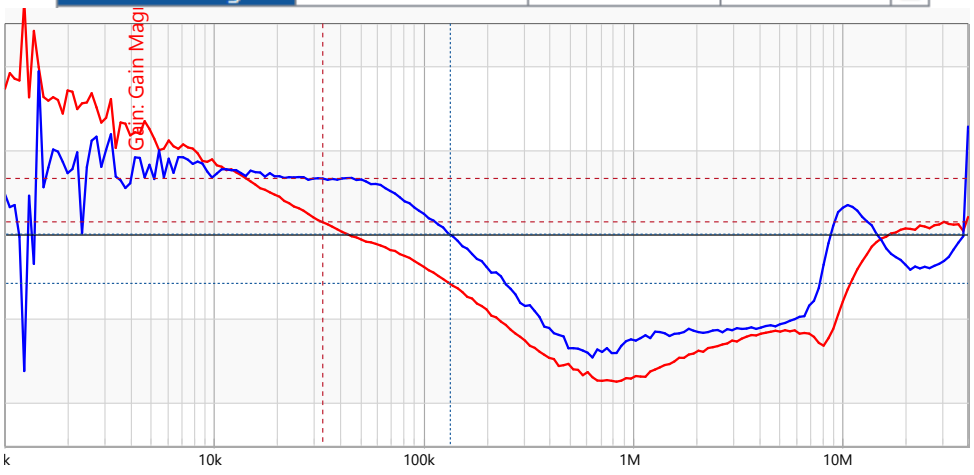
- Change the source level.



Frequency (Hz)

Gain Phase

	Frequency	Gain	Phase
Phase Margin	32.689 kHz	0 dB	59.082 °
Gain Margin	132.985 kHz	-14.195 dB	0 °



Frequency (Hz)

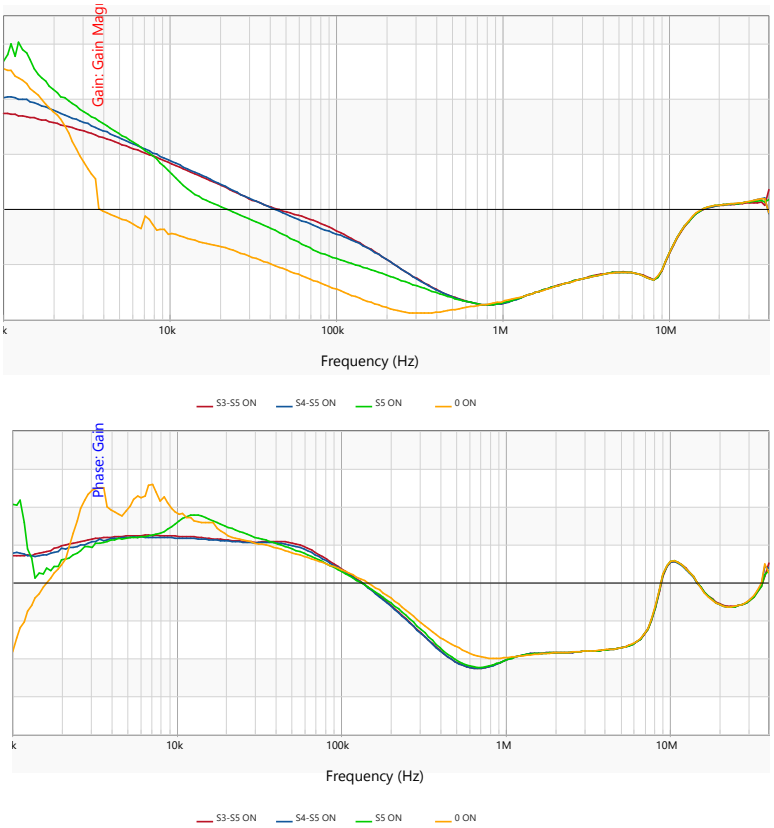
Gain Phase

	Frequency	Gain	Phase
Phase Margin	44.101 kHz	0 dB	54.214 °
Gain Margin	134.95 kHz	-11.724 dB	0 °

The top measurement is when the source level is at the Bode100's maximum which is 13dBm. The bottom measurement is when the source level is at the Bode100's minimum which is -27dBm. We also record the phase margin. Notice the changes that occur due to large signal effects.

Other Things to Try:

- Increasing the POL load.



The gain and phase measurements for the POL under different loads. Notice the change in margin with the change in load. As we increase the load, the phase margin goes down. The 0dB crossing shifts as the load increases but the phase does not change very much, thus giving a lower phase margin.

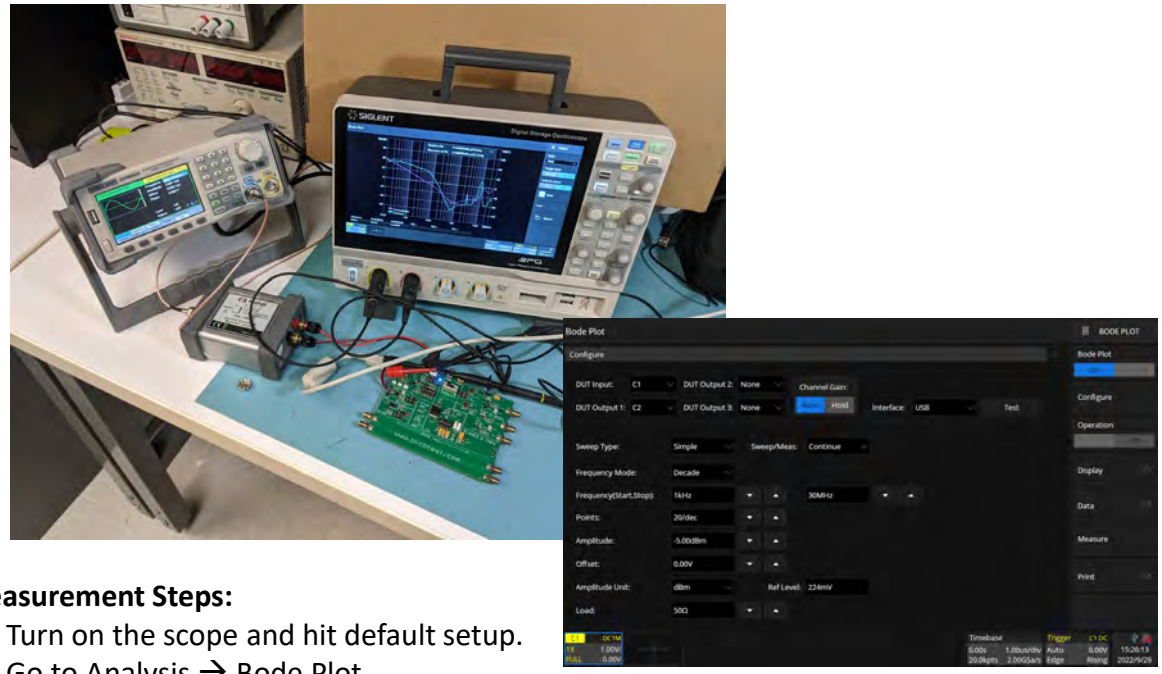
The most common error made when measuring Bode plots is that the signal is too large. Reduce the signal to the minimum level (-27dBm to -30dbm for the Bode100). The plot may still not seem exactly right. It is often necessary to further attenuate the source signal in order to maintain small signal operation. The poor measurement is NOT due to the analyzer, but due to the small signal limits of the circuit being measured. In order to assure that level is sufficiently low, increase the signal level 2dBm and check that the results have not changed. If they have, insert an attenuator, such as the J2140A between the source and the injection transformer and repeat these steps until increasing the source signal 2dBm does not change the results.

Hopefully, you know how to use the Bode100 to create a bode plot. You should also know how to find the phase margin in the bode plot. You should see that the cursor measurement and the bode plot measurement should be similar.

Other Things to Try:

- Measure the Bode plot using the Siglent scope and Siglent function generator.

Setup File: Open the setup file **bode_pol.csv**



Measurement Steps:

1. Turn on the scope and hit default setup.
2. Go to Analysis → Bode Plot
3. Go to Configure and setup the parameters. If you are connecting an external waveform generator, be sure to change input to USB
4. Hit Operation to run a measurement.
5. If you want the gain margin and phase margin, go to “Measure” and select the correct channel and measurement you want. In this case we would select C2 and the gain and phase margin.

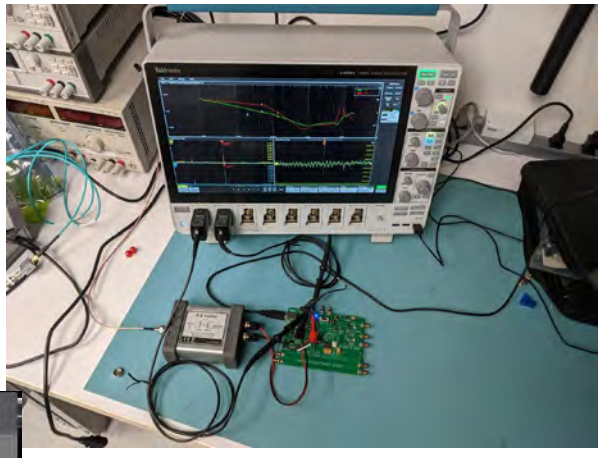
We got a phase margin of 53° which is close enough to the 56° phase margin measured by the Bode100.

Other Things to Try:

Measure the Bode plot using the MS06.

- Go to Measure → Frequency Response Analysis → Control Loop Response.
- Set the AFG using the "AFG" window.
- Set the resolution bandwidth in the "Spectrum" window.

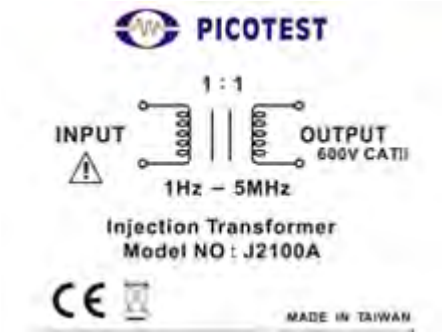
Setup File: Open the setup file **ms06 bode.tss**



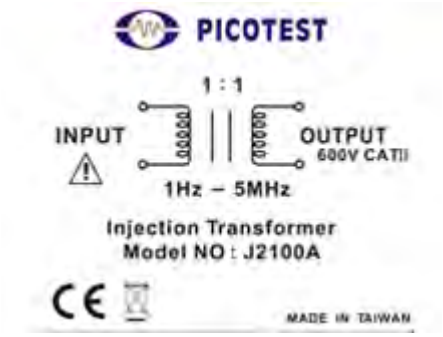
Results:

The measured Bode plot is very similar in all methods. We measured a phase margin of ~55°.

Other Things to Try:
You may have noticed that we use the J2101A injection transformer that goes from 10MHz to 45MHz. There are two other injection transformers, the J2100A and the BWIT. Let's compare them.



- **1Hz - supports PFC regulators**
- 5MHz – high enough for most power supplies and regulators
- 23 Octave range
- Low distortion for superior precision
- 5Ω termination for minimum impact to the loop
- Includes attenuation to assure small signal measurements



- **10Hz - supports off-line power supplies**
- 45MHz - high enough for even state of the art regulators
- 23 Octave range
- Low distortion for superior precision
- 5Ω termination for minimum impact to the loop
- Includes attenuation to assure small signal measurement

- **Analysis of very slow control loops (low loop bandwidth) as well as very fast control loops (high loop bandwidth)**
- 1 Hz – 10 MHz
- Highest linearity
- Low insertion loss
- 600 V CAT II isolation

Both the BWIT and the J2101A cover most applications. For most power supply bandwidths all three give the same answer.

Additional Resources (Power Integrity, pages 151-168):
https://www.picotest.com/images/download/B-WIT-Brochure_V1.1-1403.pdf
https://www.picotest.com/images/download/J2100A-J2101A_Spec_Sheet_FinalV2_Email.pdf

Voltage Reference PSRR

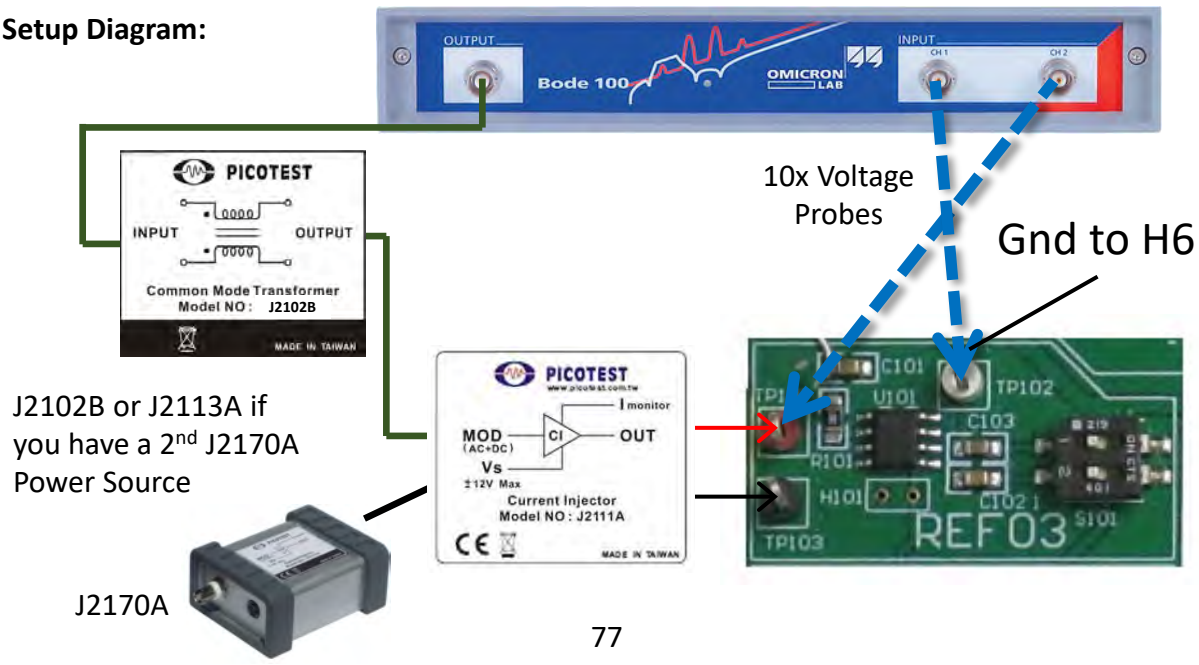
Description:
Power Supply Rejection Ratio ('PSRR') is the magnitude of the input signal divided by the output signal. The positive rejection ratio convention result is determined by the input divided by output. The input is an AC modulation signal superimposed on the voltage reference input. The output is the AC output signal of the device at the same modulation frequency. This test measures the PSRR of the REF03 voltage reference on the VRTS3 board.

Instrument	Bode 100
Injectors	J2111A Current Injector
Probe points	H6 (GND), TP101, TP103
Probes	10:1 voltage probes (2)

Setup file: Open the setup file **REF02 PSRR J2113A.bode3**
Calibration:

1. Connect the Bode 100 Output to the J2102B common mode transformer and then to the MOD port of the J2111A.
    - The J2102B is necessary to account for the ground loop that exists.
    - If you have two J2170s, use the active J2113A.
2. Set the J2111A switch to Off Bias.
3. Connect the positive output of the current injector to TP101 and the negative output to TP103.
4. Connect both CH1 and CH2 of the Bode 100 to TP101 using voltage probes (10x).
    - The ground clip of the CH1 port probe is connected to TP103 and the ground clip of the CH2 probe port is connected to H6.
5. Select "Gain/Phase" measurement and perform the THRU Gain Calibration.

Setup Diagram:



Measurement Steps:

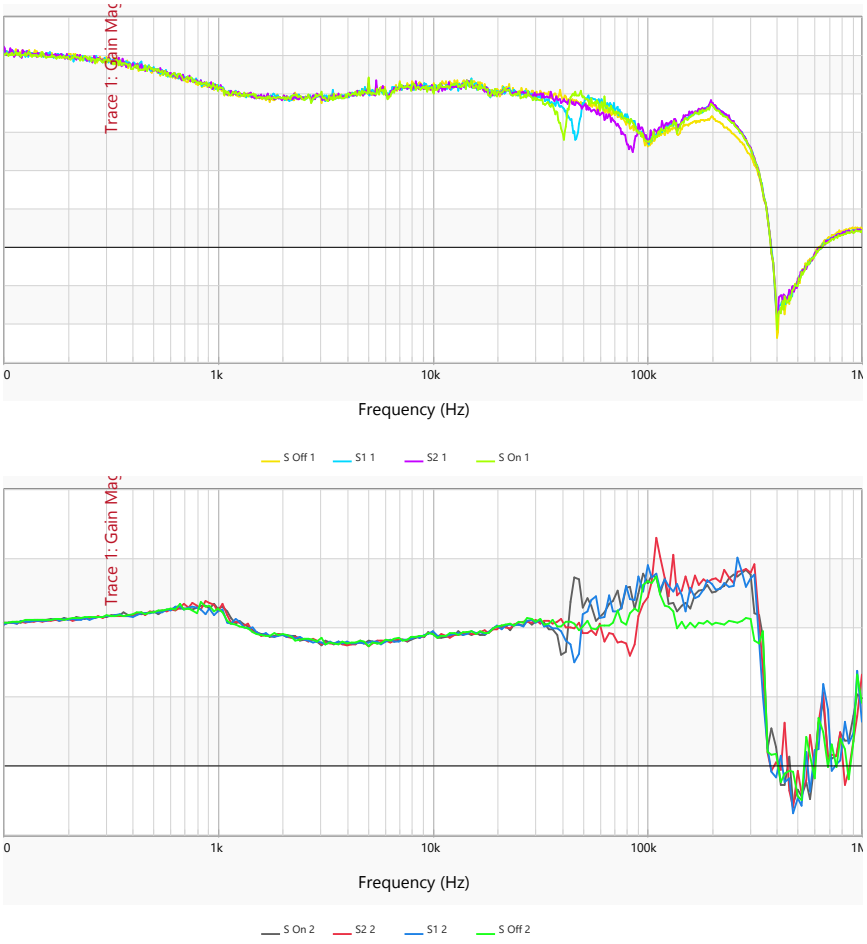
1. Connect the voltage probes to CH1 and CH2 of the Bode 100 to TP102 and TP101, respectively.
2. Trigger the measurement if needed. Trace 1 will display the PSRR.

Probe swap flips measurement from gain to attenuation

Demo Board Settings (VRTS1.5):

S1-1	S1-2	S1-3
OFF	OFF	OFF

Results:



The top graph is the PSRR measured with the J2113A Differential Amplifier. The bottom was measured with the J2102B. We also measured under different loading conditions to observe what would happen.

Hopefully, you learned how to measure the PSRR of a voltage reference. We use a current injector because we cannot break the DC source that comes from somewhere else. We need access to the input for PSRR and cannot access the input if connected to another source or regulator, therefore we use a current injector to do current modulation which will allow us to modulate a voltage signal.

Regulator Bode Plot (VRTS1P5)

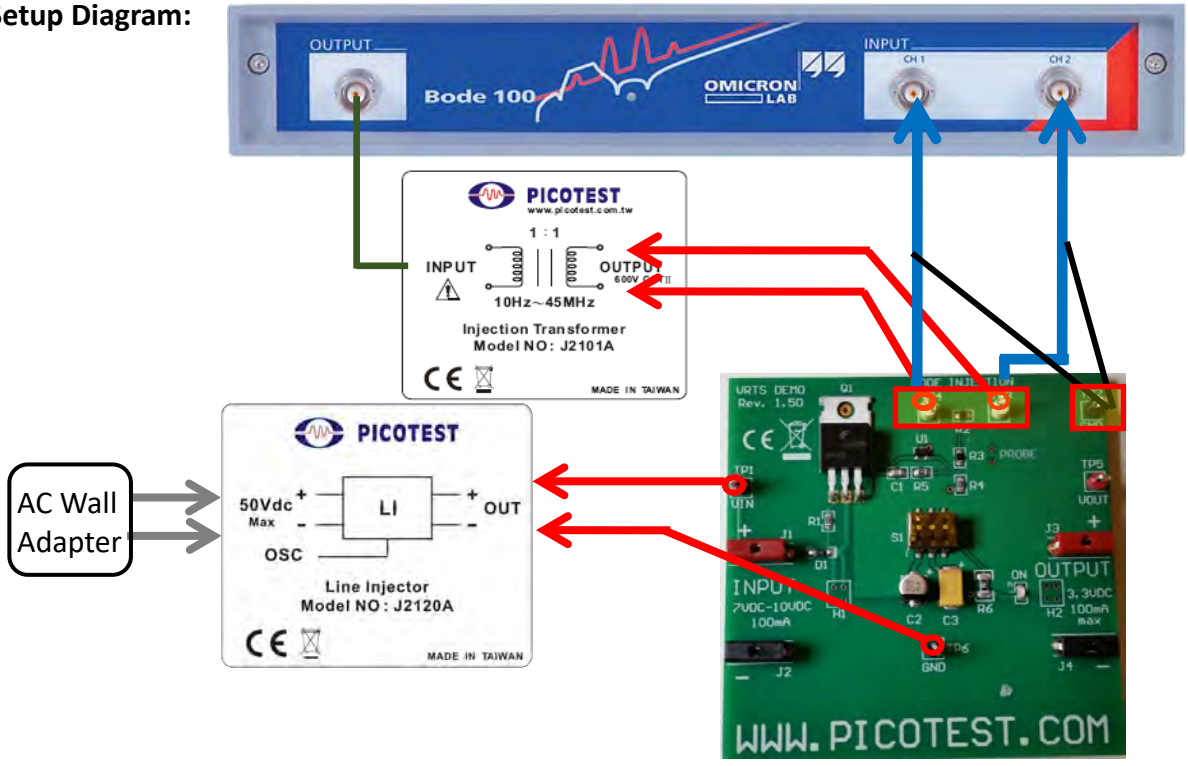
Description:
This test measures the Bode plot of the BJT voltage regulator on the VRTS1.5 board. The impact of output capacitors loading is demonstrated.

Instrument	Bode 100 VNA
Injectors	J2101A (or J2100A) Injection Transformer, J2120A Line Injector
Probe points	GND, TP4 and TP3 (BODE INJECTION)
Probes	1:1 voltage probes (2)

Setup file: Open the setup file **vrts1p5_bode.bode3**
Calibration:

1. Connect the positive OUT and negative OUT of the J2120A Line Injector to TP1 and TP6 (Vin and GND), respectively.
2. Connect the OUTPUT of the VNA to the input of the J2101A injection transformer.
3. Connect the positive output of the injection transformer to TP3 and the negative output of the injection transformer to TP4.
4. Connect the voltage probes to CH1 and CH2 of the VNA. Connect both voltage probes to either TP3 or TP4. Connect both probes to the same signal for calibration.
5. Select “Gain/Phase” measurement and perform THRU calibration.

Setup Diagram:



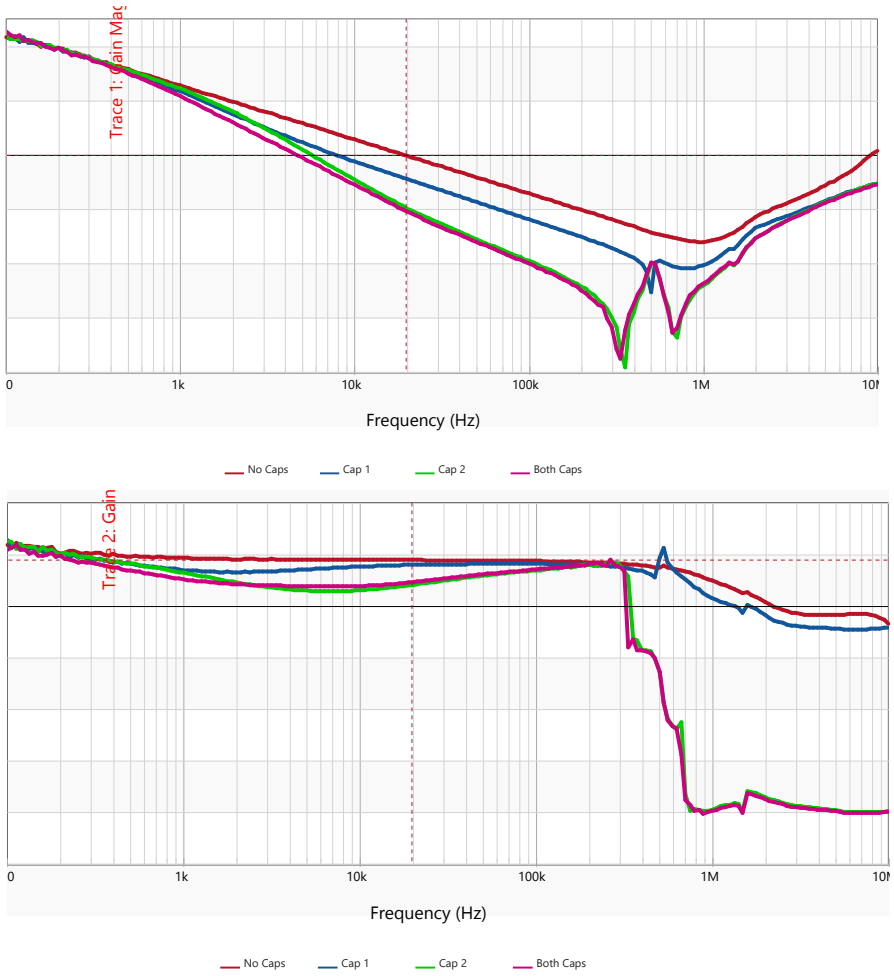
Measurement Steps:

1. Connect the voltage probes of CH1 and CH2 to TP4 and TP3, respectively. The ground clips remain on GND.
2. Trace 1 will display the gain curve of the BJT regulator Bode plot.
3. Trace 2 will display the phase curve.
4. Click the measurement icon.

Demo Board Settings (VRTS1.5):

S1-1	S1-2	S1-3
OFF	OFF	OFF

Results:



Trace 1 (top) is the gain curve of the BJT regulator Bode plot and Trace 2 (bottom) is the phase curve. Multiple curves are shown for different output capacitor loading configurations. Note that the phase margin is ~90° with No Caps and goes down as we add more capacitive loading. The 0dB shifts left and lowers the phase margin to ~40° with Both Caps.

Hopefully, you know how to measure the bode plot for a regulator. You should also get a small sense on how capacitive loading affects the phase margin.

Additional Resources (Power Integrity, pages 151-168):

http://www.aeng.com/testing.htm - Five Things Every Engineer Should Know About Bode Plots

Regulator PSRR (VRTS1P5)

Description:
Power Supply Rejection Ratio ('PSRR') is the magnitude of the input signal divided by the output signal. The positive rejection ratio convention result is determined by the input divided by output. The input is an AC modulation signal superimposed on the power supply voltage. The output is the AC output signal of the device at the same modulation frequency. This test measures the PSRR of the BJT voltage regulator on the VRTS1.5 board.

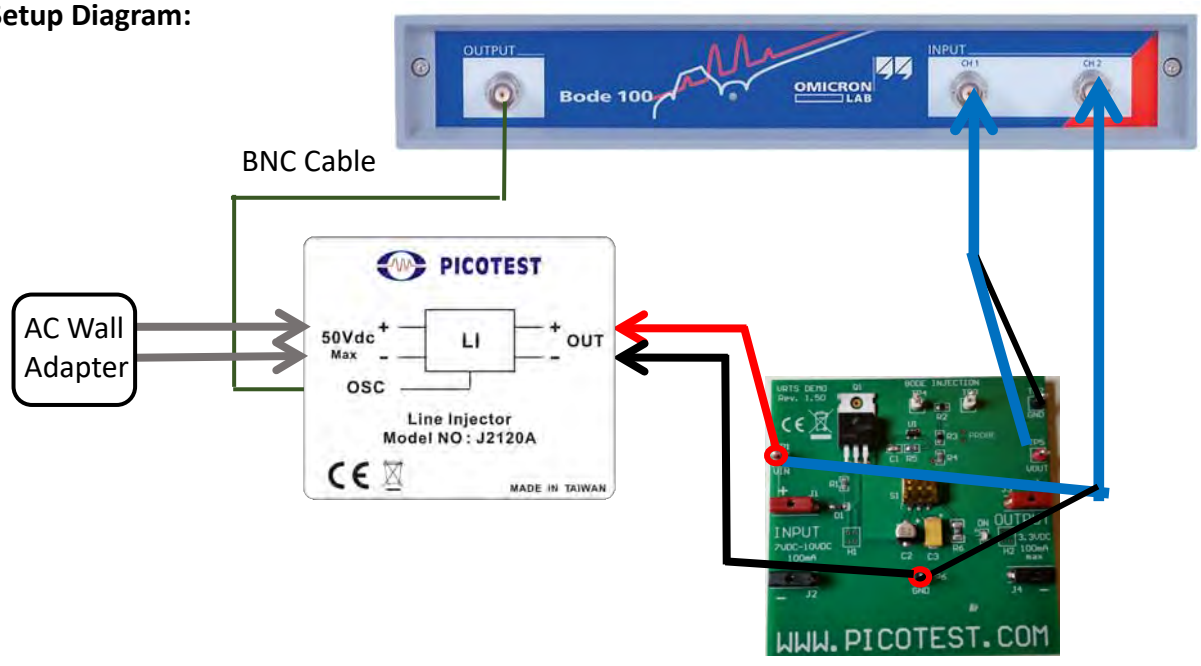
$$PSRR = \frac{\Delta Vin}{\Delta Vout}$$

Instrument	Bode 100 VNA
Injectors	J2120A Line Injector
Probe point	TP1, TP2, TP5, TP6
Probes	1:1 voltage probes (2)

Setup file: Open the setup file **vrts1p5_psrr.bode3**
Calibration:

1. Connect the OUTPUT of the VNA to the OSC port of the J2120A.
2. Connect the positive OUT and negative OUT of the J2120A to TP1 and TP6 (Vin and Gnd), respectively.
3. Connect both CH1 and CH2 of the VNA to TP1 using voltage probes.
4. Connect the ground clips of the voltage probes of CH1 and CH2 to TP6 and TP2.
5. Select the "Gain/Phase" measurement.
6. Perform the THRU Gain/Phase Calibration.

Setup Diagram:



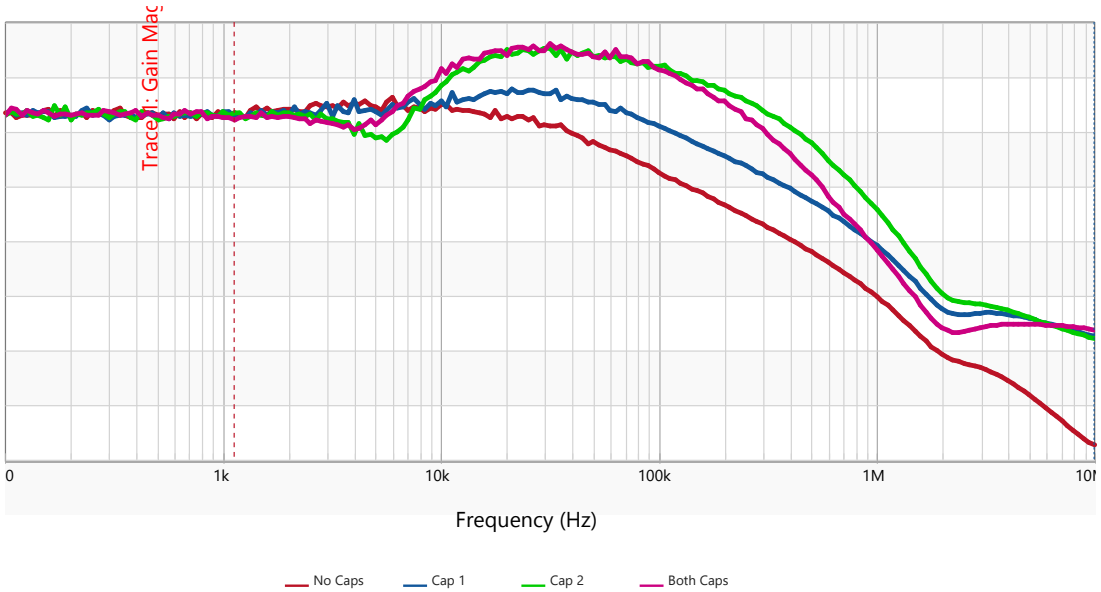
Measurement Steps:

1. Connect the voltage probes of CH1 and CH2 to TP5 (output) and TP1 (input), respectively.
2. The ground clips of the voltage probes of CH1 and CH2 remain at TP6 and TP2, respectively.
3. Trace 1 will display the PSRR of the BJT voltage regulator.
4. Click the measurement icon.

Demo Board Settings (VRTS1.5):

S1-1	S1-2	S1-3
OFF	OFF	OFF

Results:



The PSRR measurement of the BJT voltage regulator is shown above for multiple capacitor loading configurations.

Hopefully, you know how to measure the PSRR of a regulator.

Additional Resources (Power Integrity, pages 181-199):

https://www.picotest.com/blog/?p=610 - Measuring the PSRR of Voltage References
https://www.picotest.com/blog/?p=839 - Measuring Op Amp PSRR
https://www.picotest.com/blog/?p=364 - Step-by-Step Guide to Measuring PSRR
https://www.picotest.com/blog/?p=432 – Video, PSRR Measurement using the J2120A Line Injector

POL Switching Regulator Step Load

Description:
This test measures the step load response of a 2.9MHz switching POL regulator.

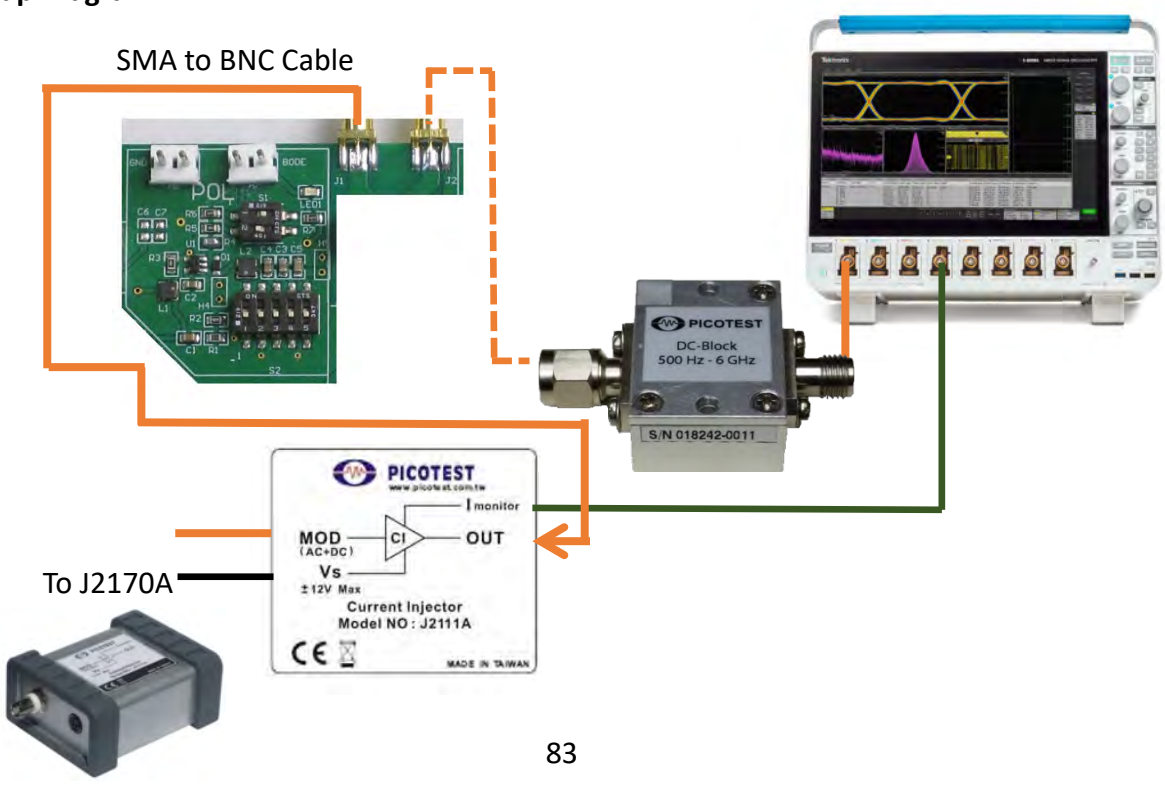
Instrument	Oscilloscope
Injectors	J2111A Current Injector, P2130A DC Blocker, J2170A High PSRR Adapter, Picotest Harmonic Comb
Probe point	J1, J2
Probes	N/A

Setup file: Open the setup file **pol step load.tss**
Measurement Steps:

1. Set the switches to the configuration shown above.
2. Connect the Function Generator to the MOD of the J2111A.
3. Connect the Vs of the J2111A to the J2170A.
4. Connect I_monitor of the J2111A to CH3 of the oscilloscope.
5. Connect J1 to the OUT of the J2111A.
6. Connect J2 to CH1 of the oscilloscope via the P2130A.
    - CH1 is the output voltage and CH5 is the applied load step.
7. The step load response should appear on the oscilloscope screen once the load step is applied using the Harmonic Comb.

Setup Diagram:

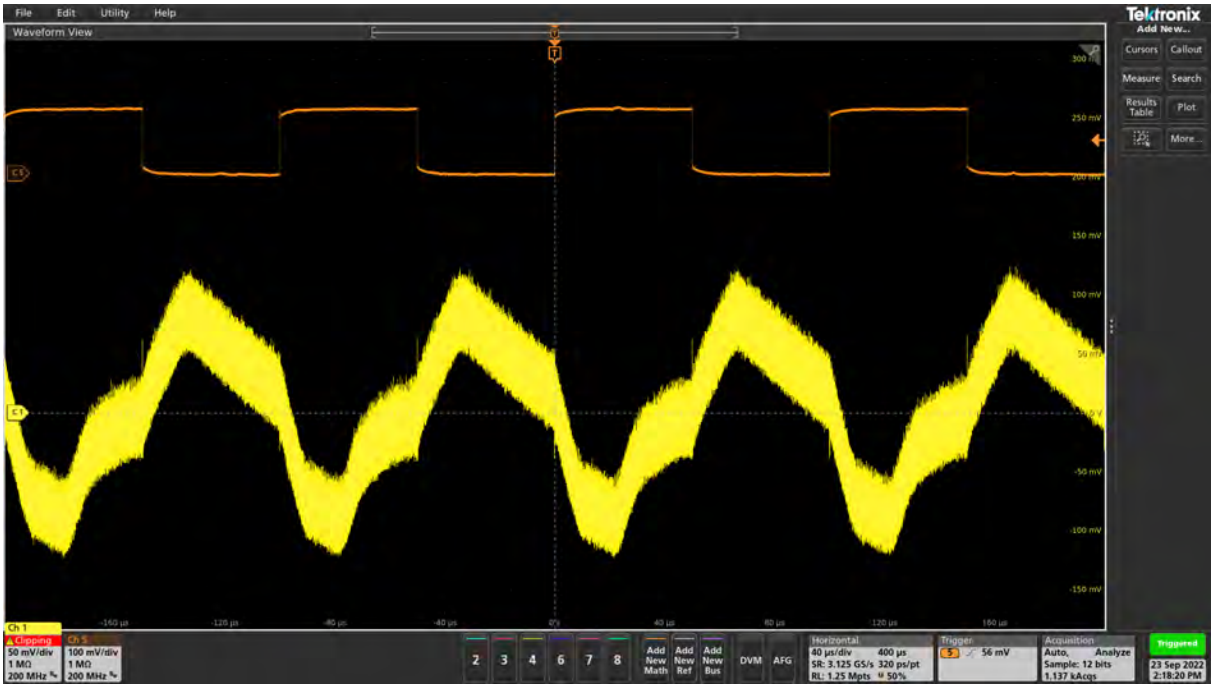
CH1 is set to 50Ω DC
CH5 is set to 50Ω DC



Demo Board Settings:

S2-1	S2-2	S2-3	S2-4	S2-5	SEL1	USB	S1-1	S1-2	S401-1	S401-2
OFF	OFF	OFF	OFF	OFF	LEFT	ON	ON	OFF	OFF	OFF

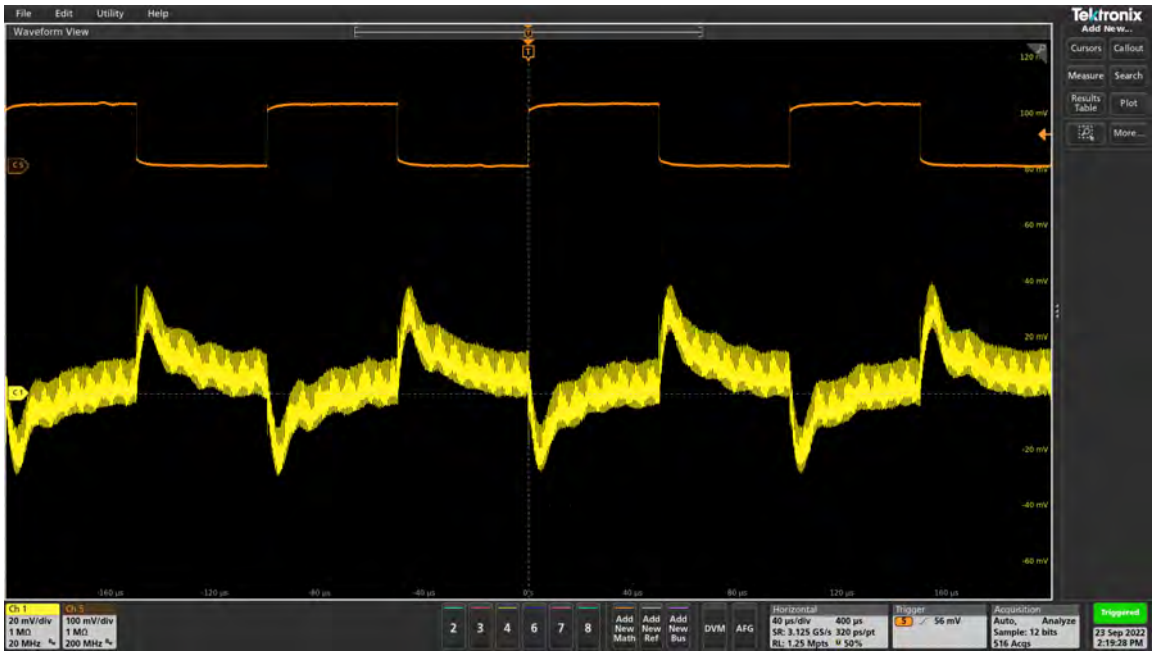
Results:



The step load response is shown on CH1 and the applied load step is shown on CH3. The amount of low frequency ringing is related to the stability of the system.

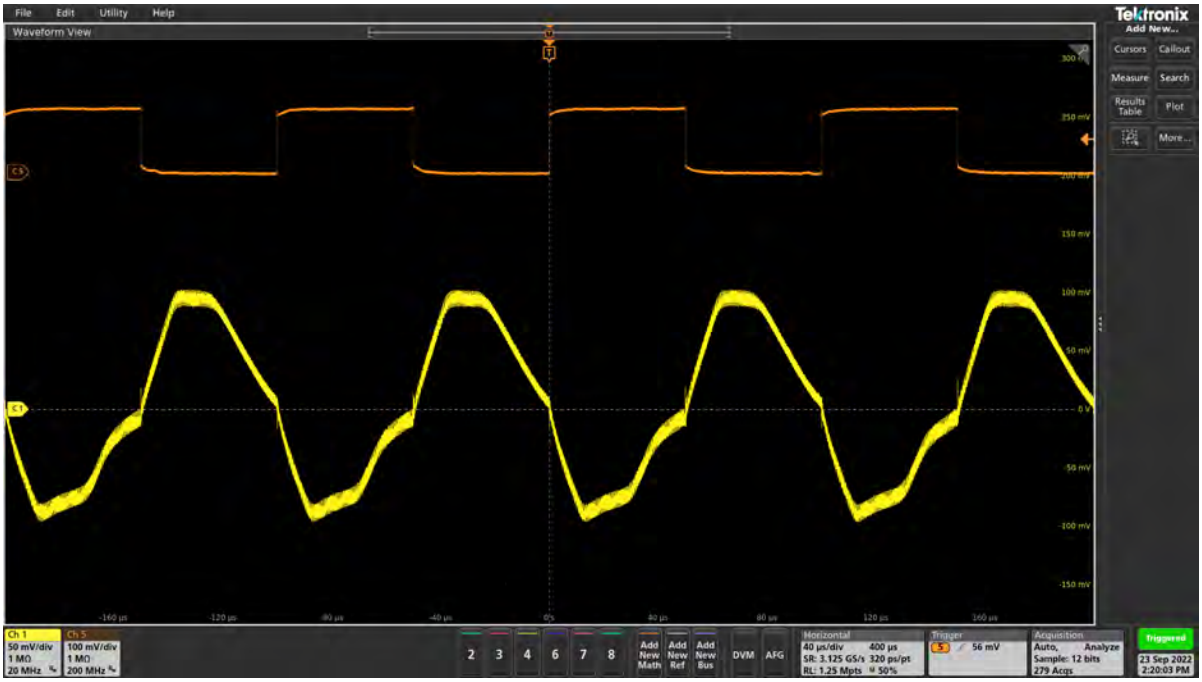
Other things to try:

- Flip all the S2 switches up so that they are ON.

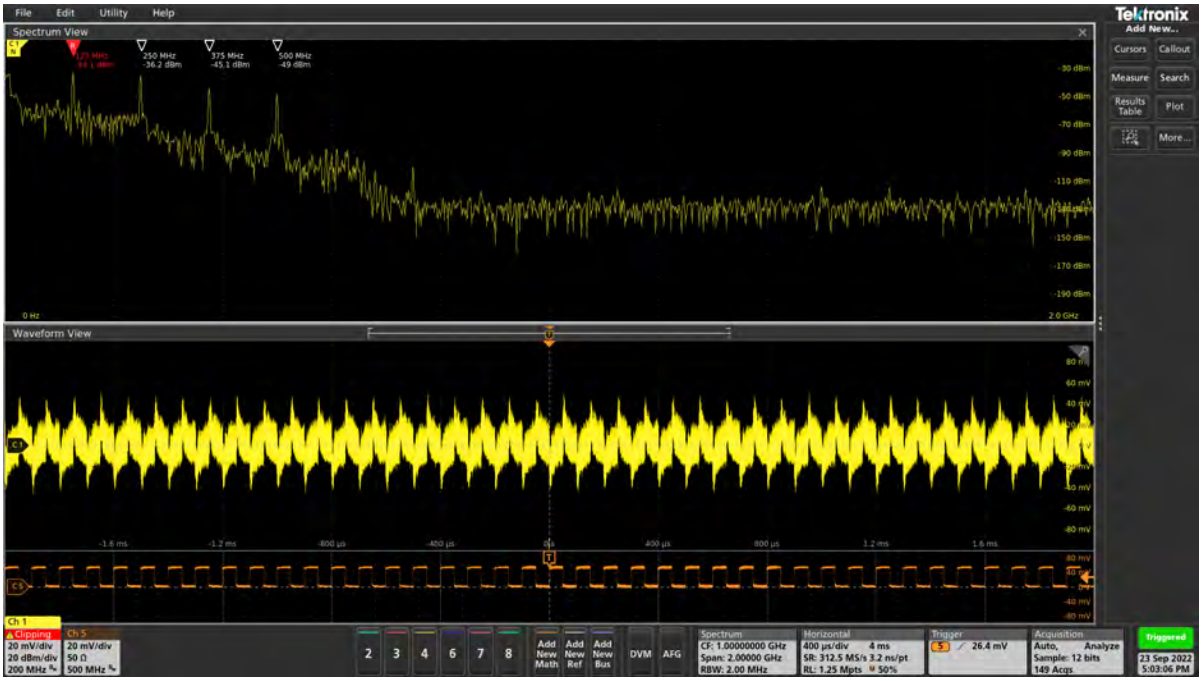


Other things to try:

- Flip S401-1 to its ON position.



- Look at the ripple spectrum.



Hopefully, you know how to measure the step load of a POL.

Additional Resources (Power Integrity, pages 217-232):

POL Input Capacitor Ripple

Description:
A periodic variation in output voltage resulting from an expected event is called ripple. For example, the switching action of a switching power supply is expected to result in an output ripple voltage. The rectification of the AC mains is expected to result in an input ripple signal. While the ripple may not be at a fixed or specific frequency, for example in a frequency modulated resonant converter, the ripple is an expected result. This test measures the input ripple of the POL across C2.

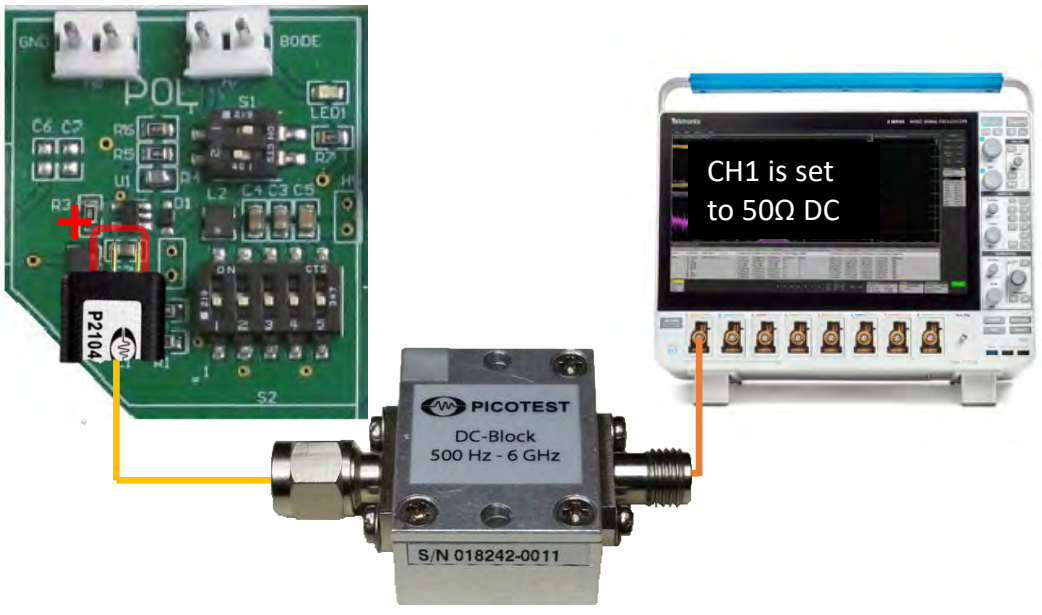
Instrument	Oscilloscope
Injectors	P2130A DC Blocker
Probe points	C2
Probes	P2104A 1-port probe (100 mil header)

Setup file: Open the setup file **cap ripple.tss**
Measurement Steps:
1. Connect the 1 port probe to CH1 using the P2130A.
2. Probe C2 using the 1 port probe in order to measure the input ripple.
3. CH1 displays the ripple across C2.

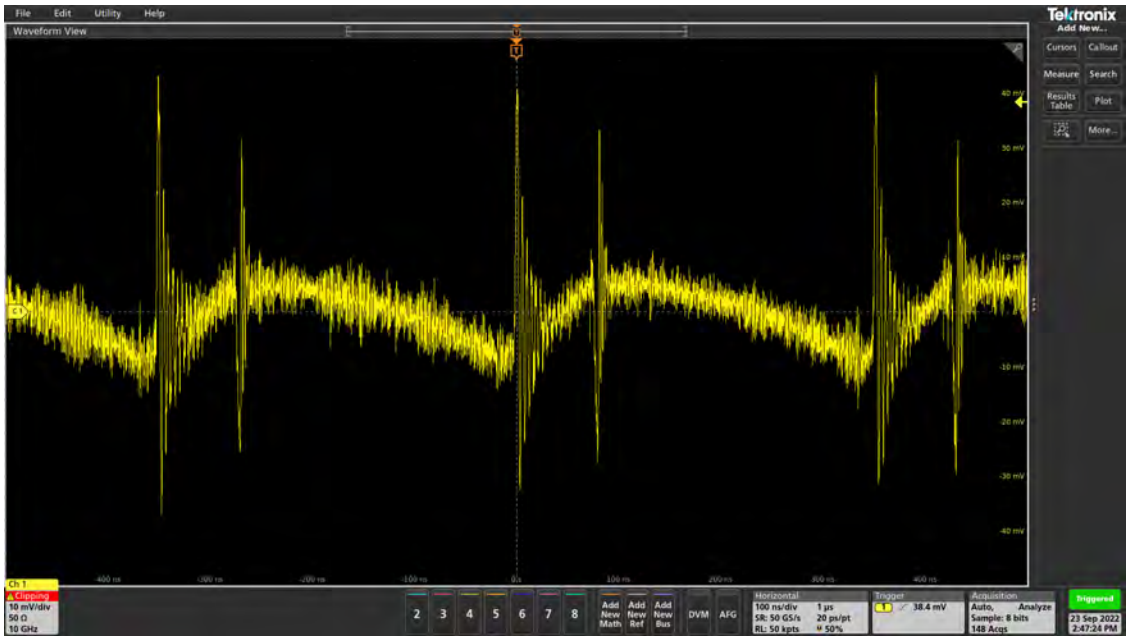
Demo Board Settings:

S2-1	S2-2	S2-3	S2-4	S2-5	SEL1	USB	S1-1	S1-2
ON	OFF	ON	ON	ON	LEFT	ON	ON	OFF

Setup Diagram:



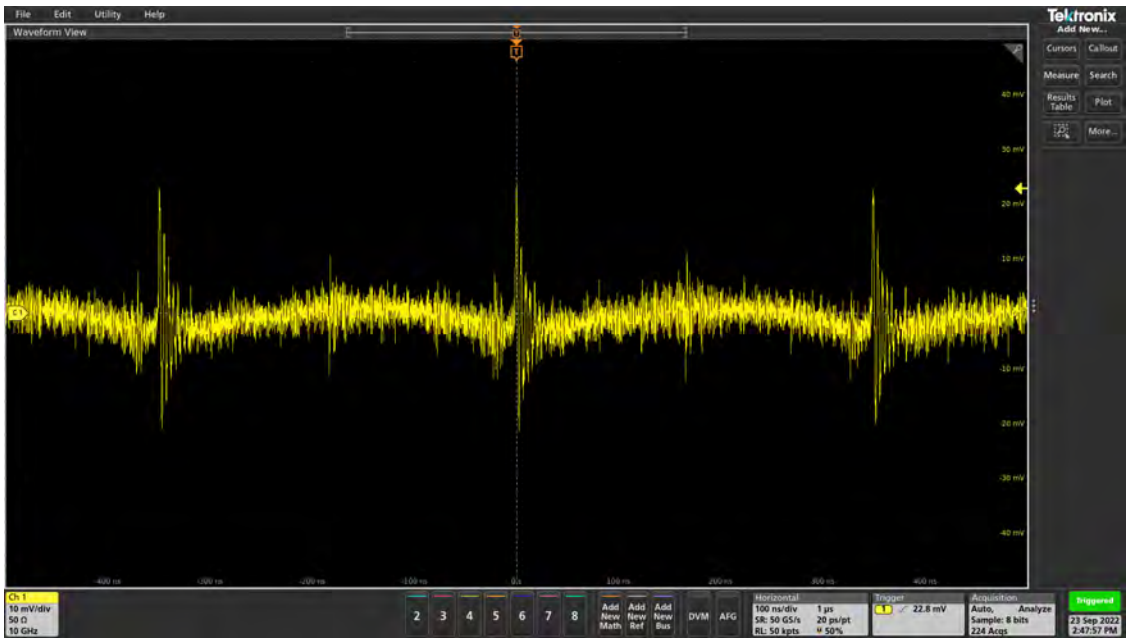
Results:



The input ripple is measured through the capacitor, C2.

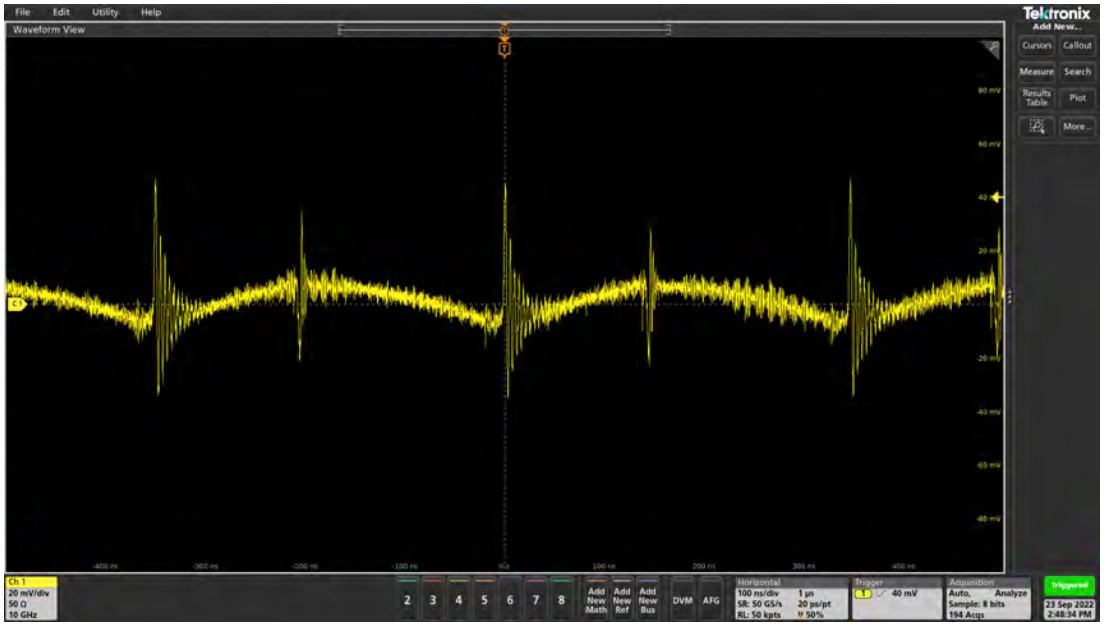
Other things to try:

- Flip all the S2 switches down so that they are OFF.

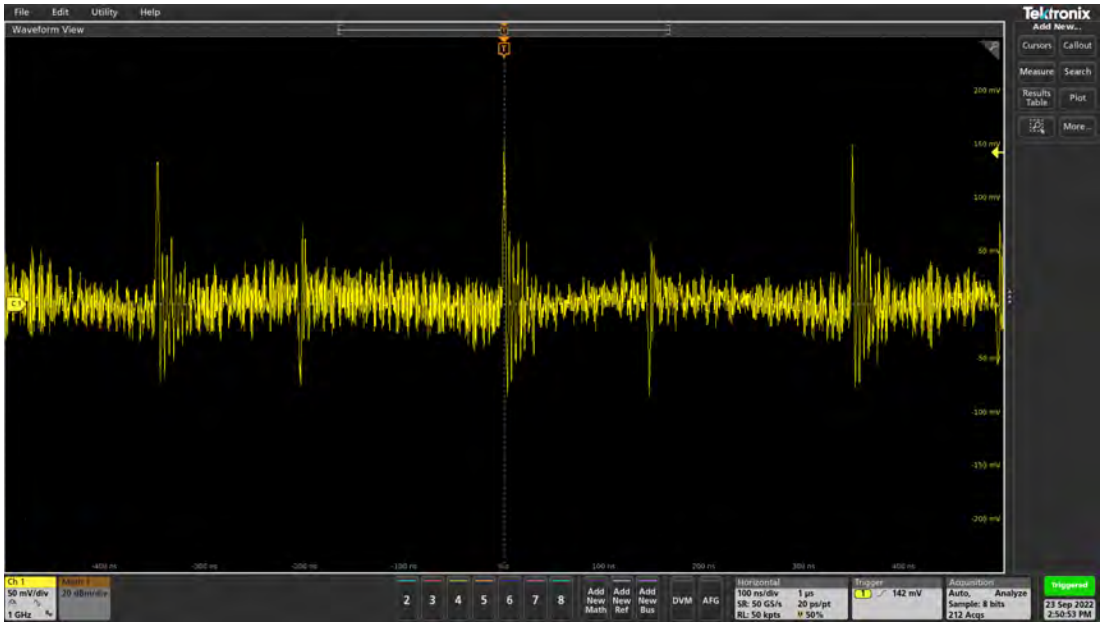


Other things to try:

- Flip S1 switches to the right in their ON position.



- Use a voltage probe and make the same measurement.



Hopefully, you now know how to measure the capacitor ripple or ripple in general. The ripple is an important measurement which can allow us to see the swing of the power signal. It allows us to see to what extent is the range of the ripple. Now that we can measure it, we can quantify whether it satisfies the specification requirements.

Additional Resources (Power Integrity, pages 223-252):

POL Ripple and Noise

Description:
This test measures the POL ripple in the time and spectrum domains.

Instrument	Oscilloscope
Injectors	P2130A DC Blocker
Probe point	H5
Probes	1 Port Probe, 10:1 Voltage Probe

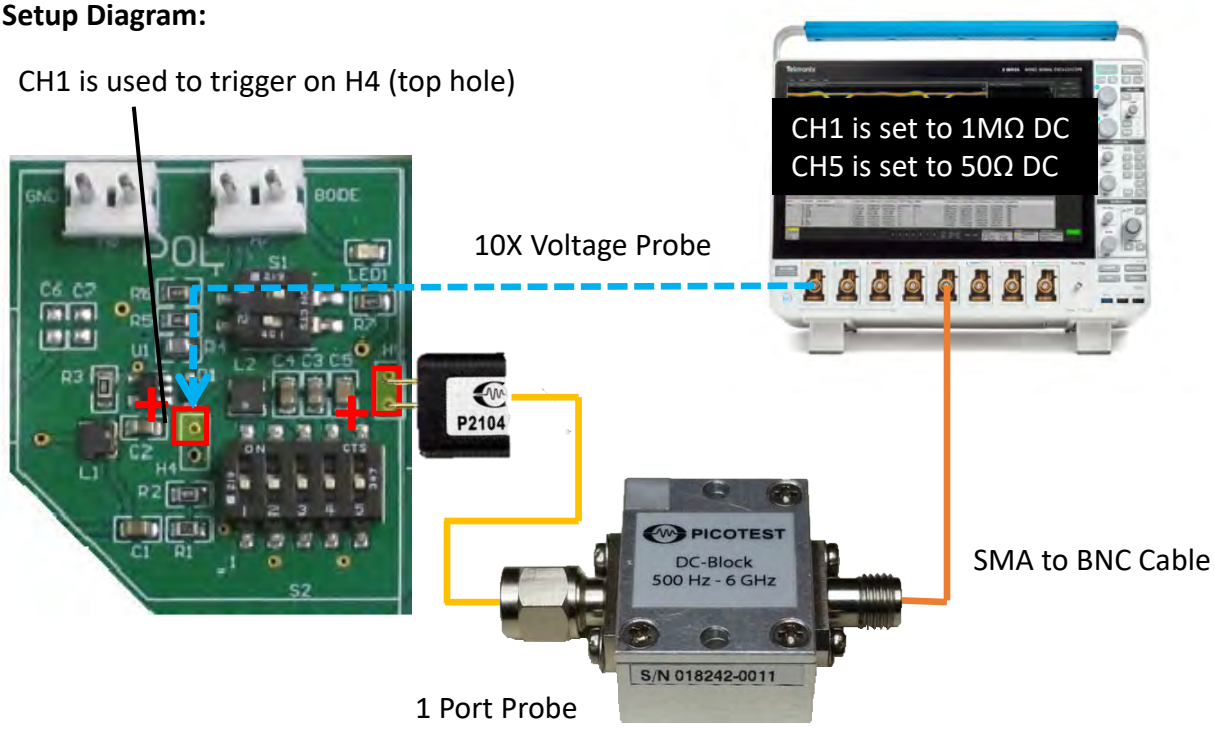
Setup file: Open the setup file **ripple and noise.tss**
Measurement Steps:

1. Connect the voltage probe (10:1) to CH1 of the oscilloscope.
2. CH1 is used as a trigger.
3. Connect the 1 port probe to CH5 of the oscilloscope using a P2130A.
4. CH5 displays the POL ripple.
5. Probe H4 using the voltage probe connected to CH1 using ground spring tip.
6. Probe H5 using the 1 port probe connect to CH1 in order to measure the POL ripple.

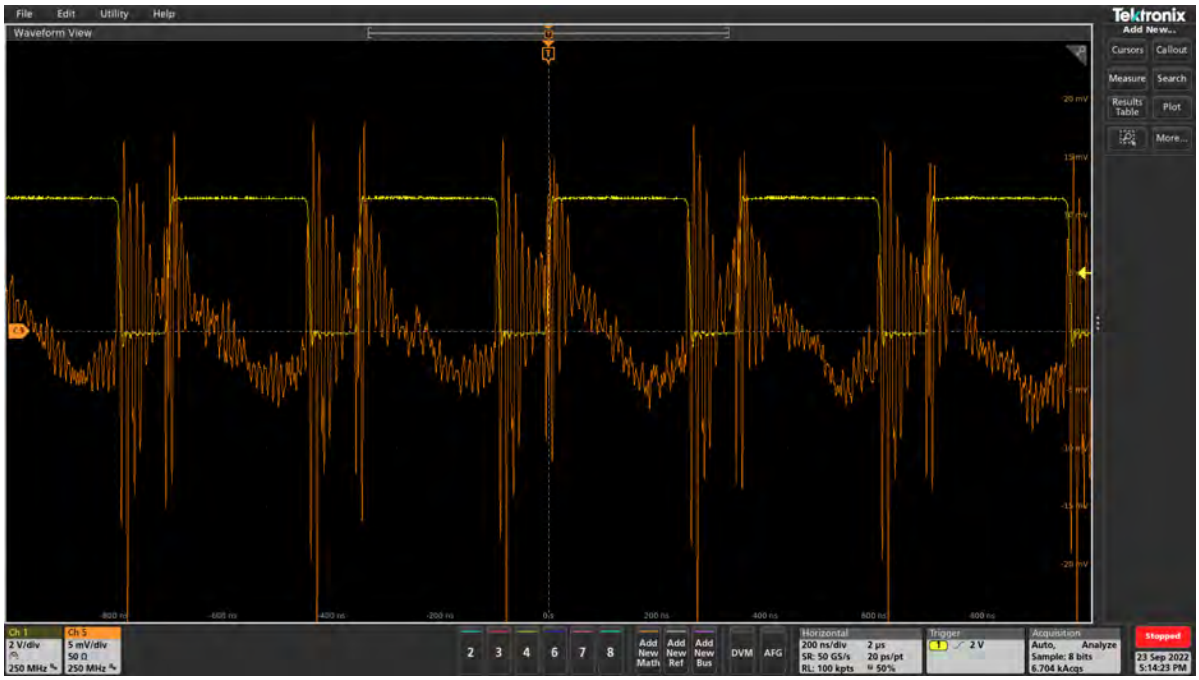
Demo Board Settings:

S2-1	S2-2	S2-3	S2-4	S2-5	SEL1	USB	S1-1	S1-2	S401-1	S401-2
ON	OFF	ON	ON	ON	LEFT	ON	ON	OFF	ON	ON

Setup Diagram:

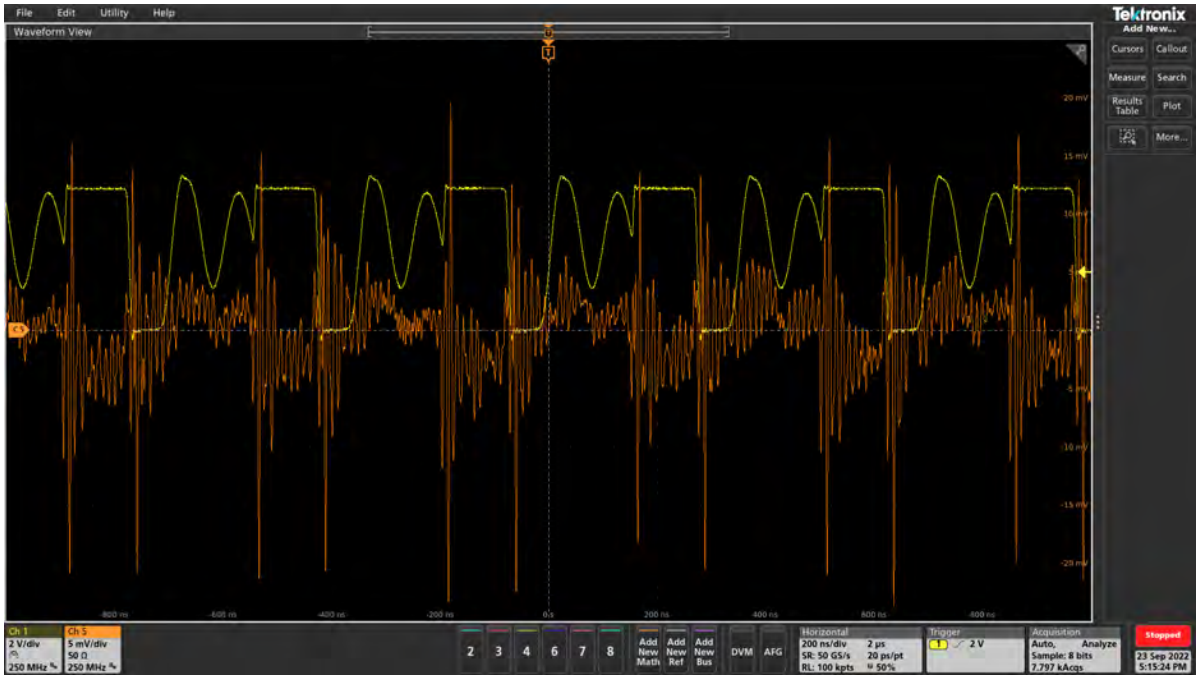


Results:



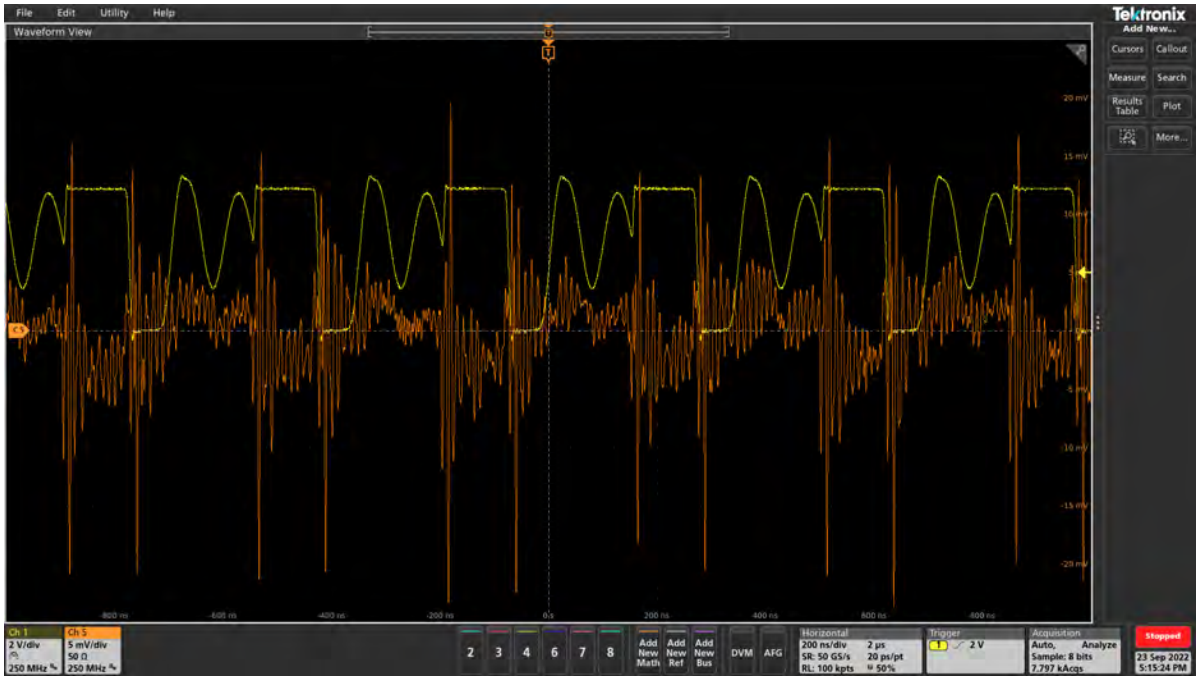
Other things to try:

- Flip all S2 switches to down to the OFF position.



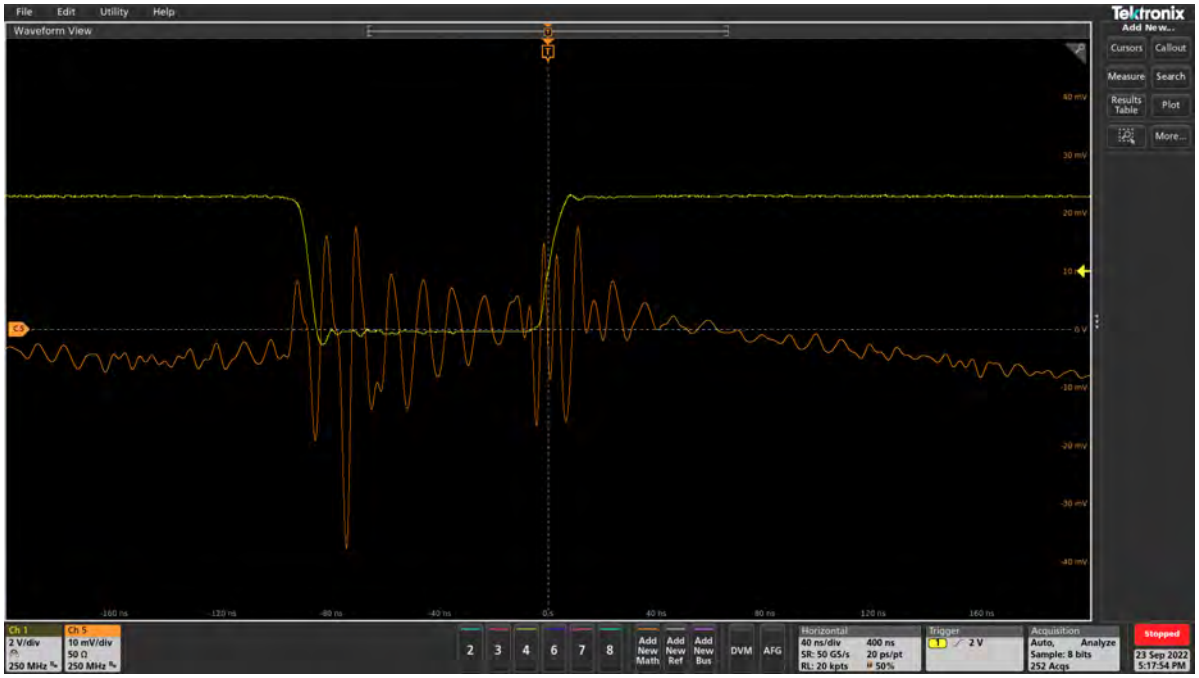
Other things to try:

- Flip all S1 switches to right to the ON position.



Other things to try:

- Zoom in on the ripple.



Hopefully now you know how to measure the ripple of a POL with a step. We can also observe the noise that occurs.

Additional Resources: Power Integrity (pages 233-252)

https://www.picotest.com/blog/?p=1009 - Making Ripple Measurements

POL EMI-Near Field Probe

Description:
EMI compliance testing consists of a far field emissions measurement. There is no definitive relationship between near and far field measurements. Though near field measurements generally don't directly correlate with far field measurements, the near field measurement is still an excellent troubleshooting tool. Near field measurements can help in identifying ground plane gaps, as well as locating leaks in enclosures, connectors and EMI seals. It can also be used to identify source characteristics that can be used to determine the source of the emissions in a subsequent far field measurement. This demonstration will measure the EMI emissions over the POL circuit.

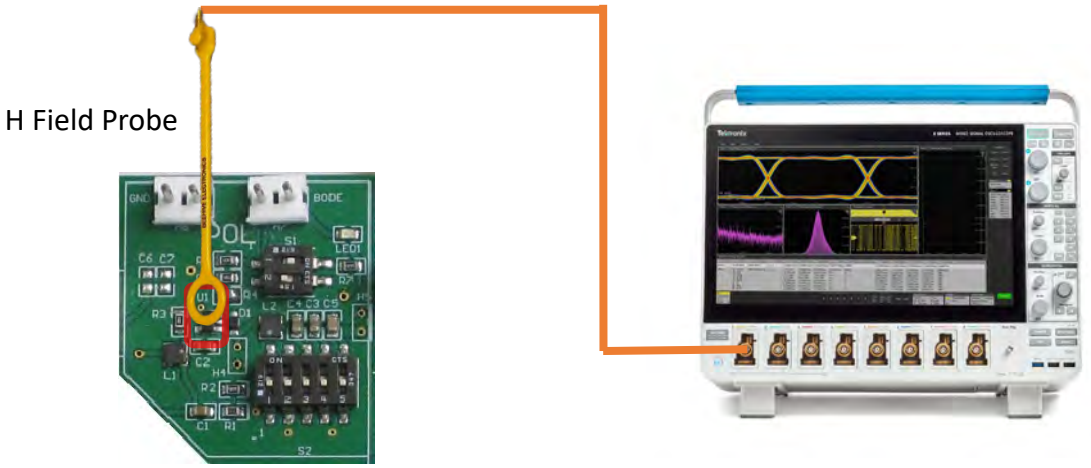
Instrument	Oscilloscope
Injectors	P2130A DC Blocker
Probe point	H5
Probes	1 Port Probe, 10:1 Voltage Probe

Setup file: Open the setup file **h field probe.tss**
Measurement Steps:
1. Setup the experiment.
2. Move the H field probe above U1 of the POL.
3. Hold the probe perpendicular to the part.
4. Look at the spectrum analyzer results on the oscilloscope.

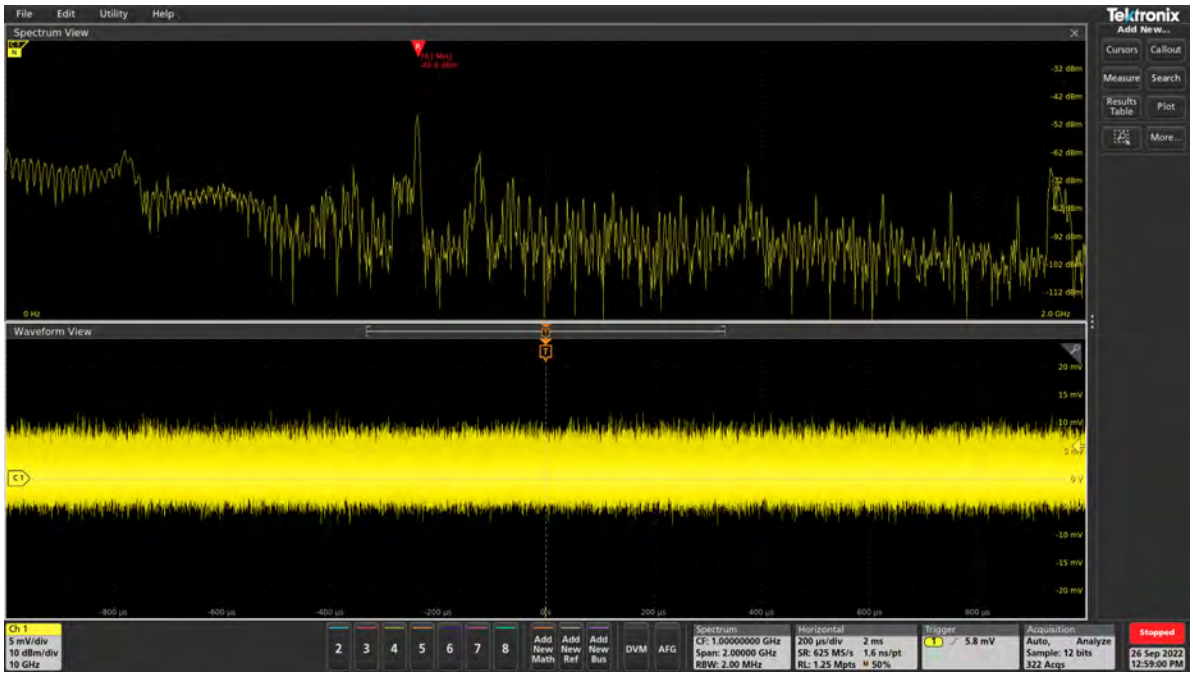
Demo Board Settings:

S2-1	S2-2	S2-3	S2-4	S2-5	SEL1	USB	S1-1	S1-2	S401-1	S401-2
ON	OFF	ON	ON	ON	LEFT	ON	ON	OFF	OFF	OFF

Setup Diagram:

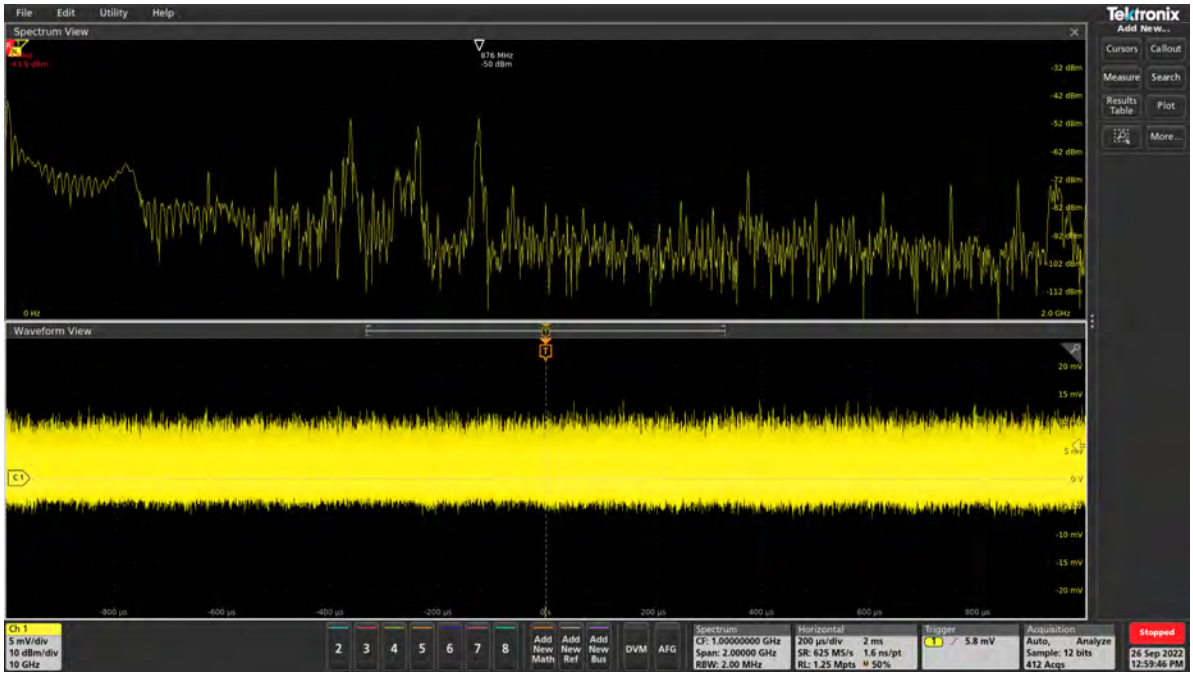


Results:



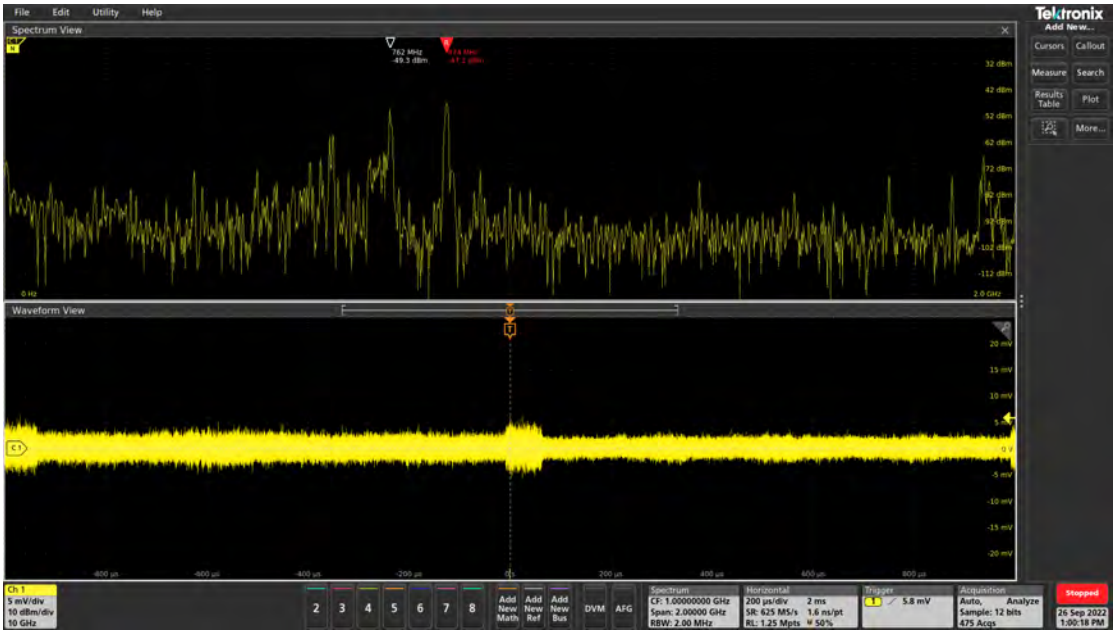
Other things to try:

- Repeat the measurement for the H probe over D1 on the board

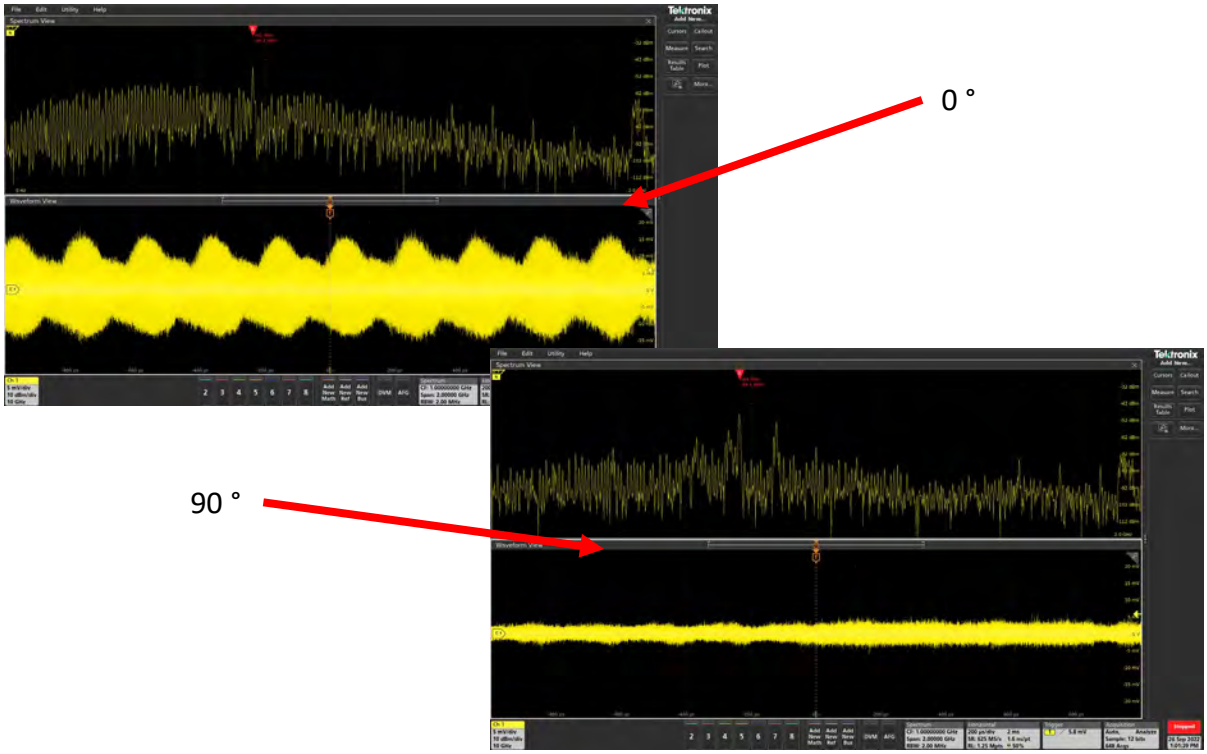


Other things to try:

- Repeat the measurement by holding the H probe between and near D1 and L2



- Repeat measurement by holding the H probe near the clocks and buffers like C408. Rotate the probe 90° and measure again.



Hopefully, you know how to use a H field probe to make a measurement. The H field probe is not ideal but can give us enough detail to make a quick and okay judgement if other methods or measurements cannot be done.

Additional Resources: Power Integrity (page 275-295).

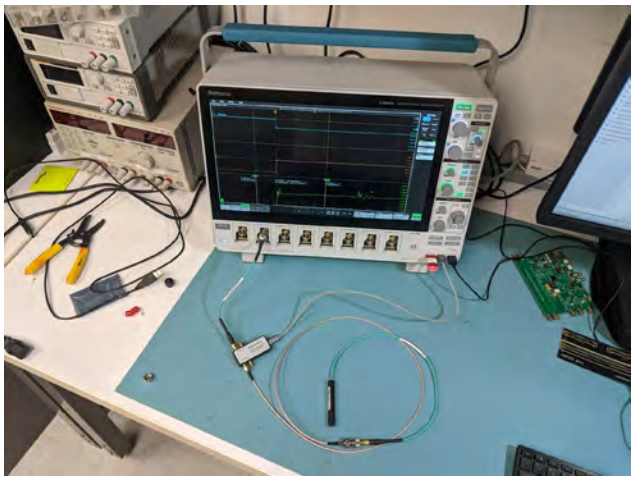
Time Doman Reflectometry (TDR)

Description:
TDR measures the impedance of the signal path via signal reflections. Discontinuities, added components, or other changes to the signal path can change the capacitance or inductance and hence the impedance of the path. These can be seen using the J2154A PerfectPulse® Differential TDR and the P2105A TDR Probe.

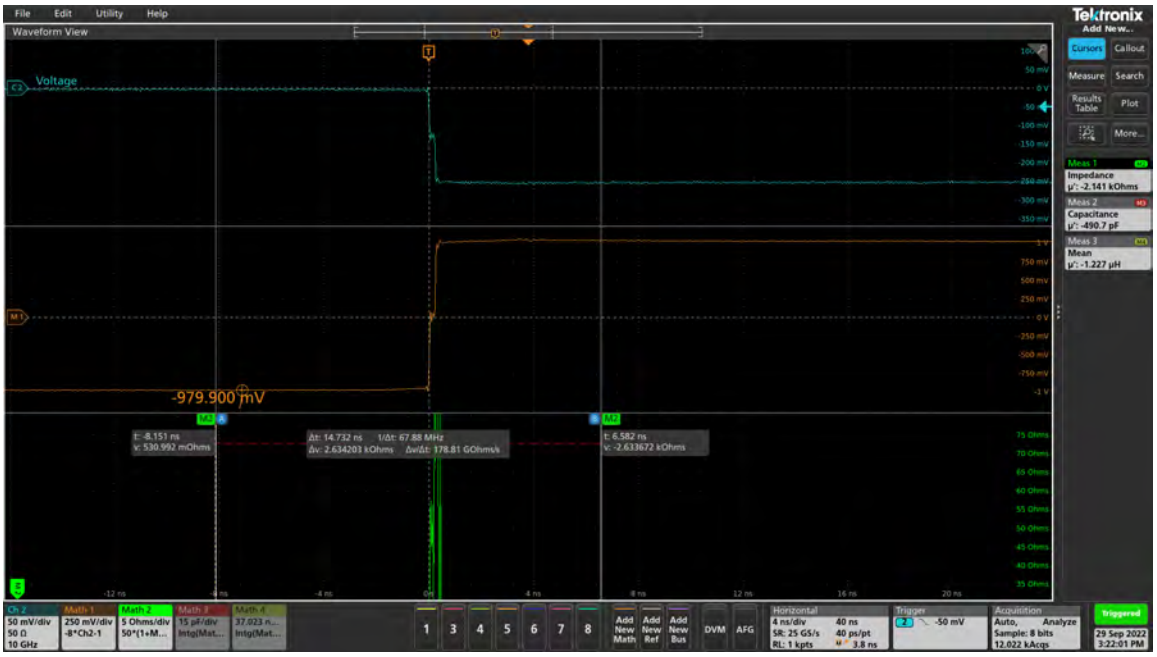
Instrument	Oscilloscope, TDR Demo Board
Injectors	J2154A
Probe points	TP1, TP3, and TP5 on the TDR Demo Board
Probes	P2105A

Setup file: Open the setup file **tdr.tss** or **J2154A single ended.set**
Measurement Steps:
1. Setup the experiment
2. Attach cable to the open end. Observe the change in the waveform.
3. Attach a connector to end of cable. Observe the change in the waveform.
4. Attach the probe to the connector. Observe the changes in the waveform.

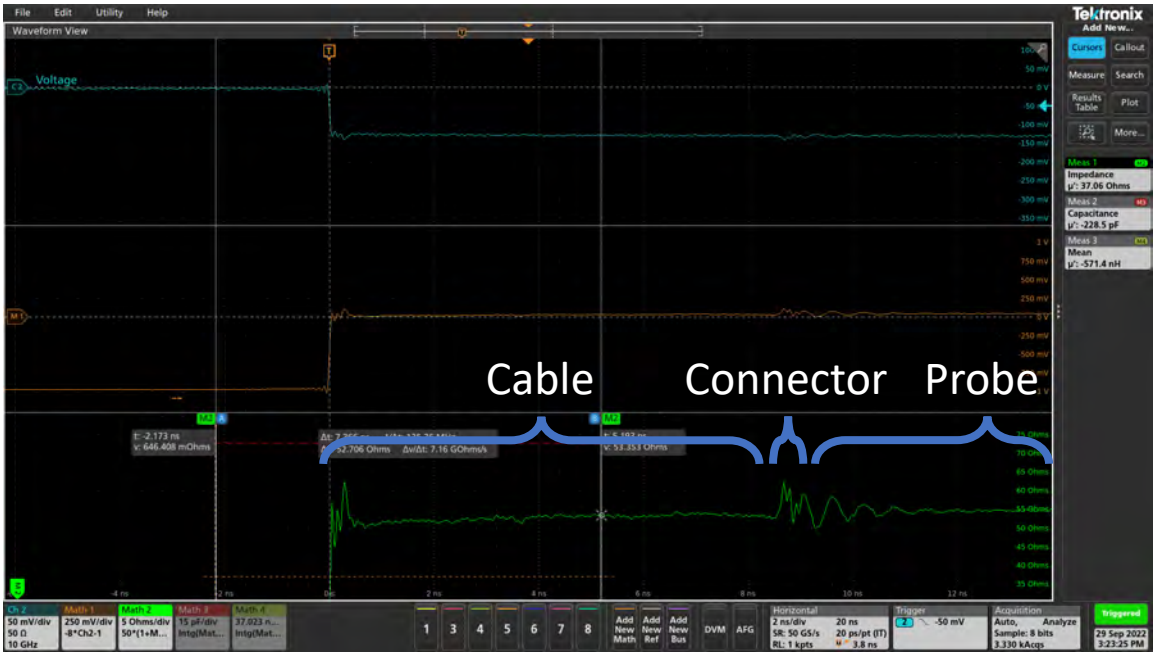
Setup Diagram:



Results:



When nothing is connected to the TDR

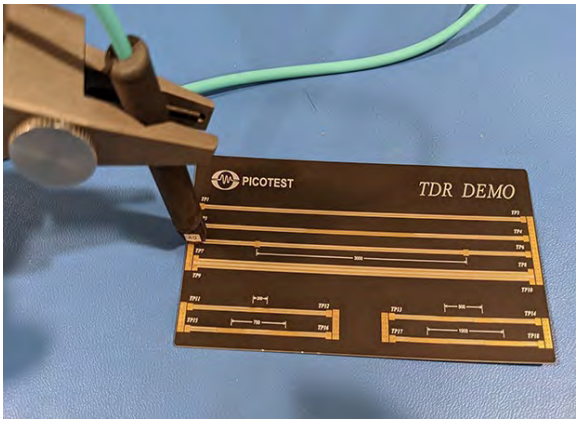


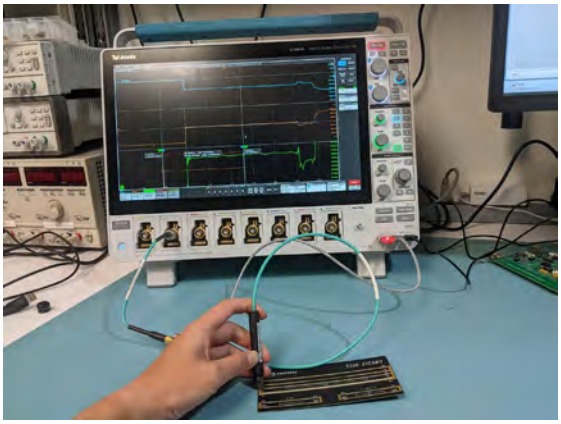
Cable, connector, and probe connected to the TDR

Through the TDR, we can see the connections and any problems/discontinuities that are in the setup. We can also see the length of the cable and the probe. We can determine the impedance of the setup and where the problems could be.

Other things to try:

- If we can do this for cables, it should work for PCB traces. Take the probe that we attached and the TDR demo board and observe the measure the PCB traces using the TDR.

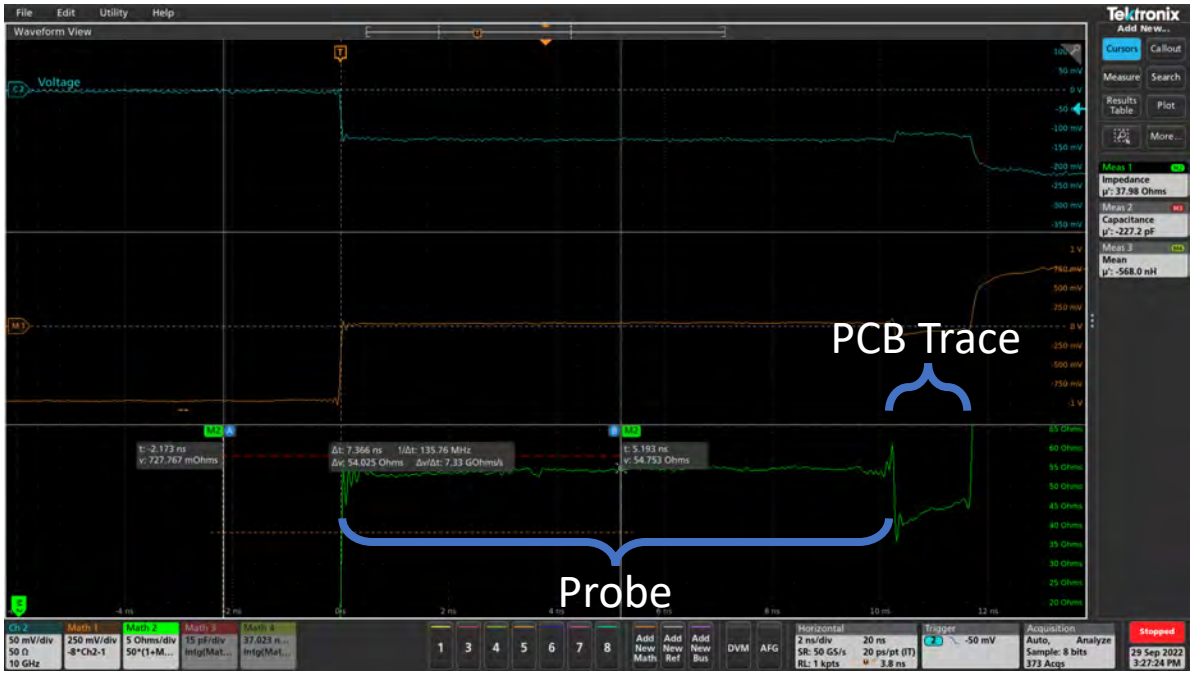




Setup Diagram:

Other things to try:

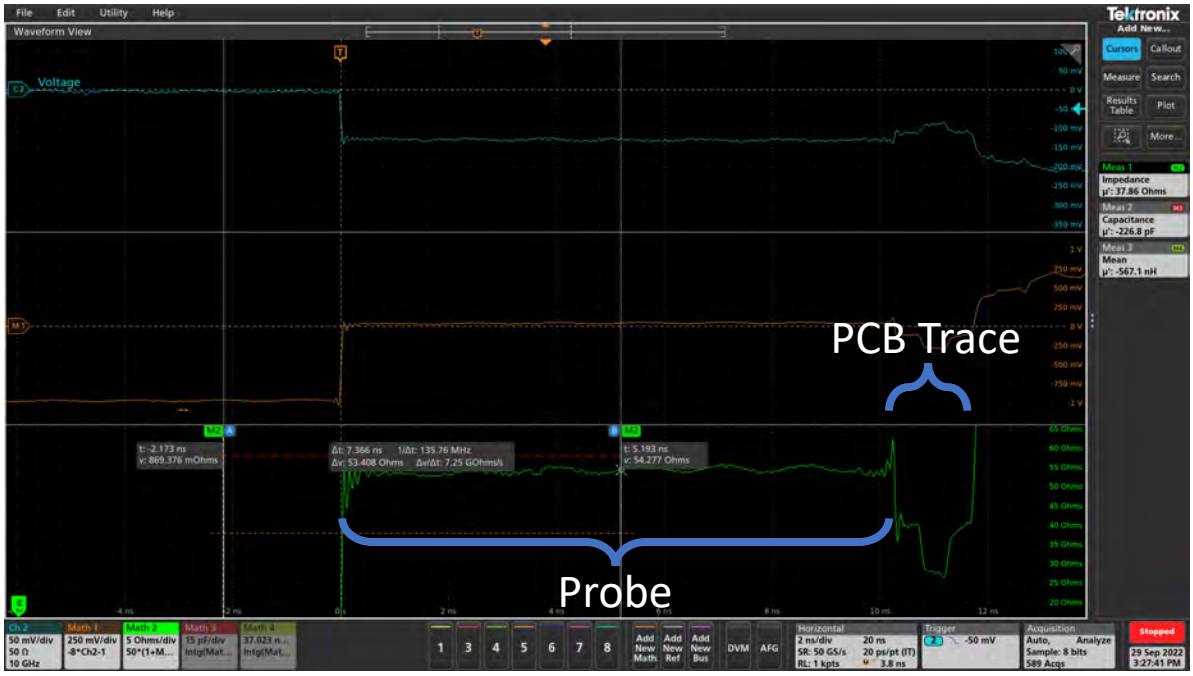
- If we can do this for cables, it should work for PCB traces. Take the probe that we attached and the TDR demo board and observe the measure the PCB traces using the TDR.



TDR Probe measurement of TP1. It is linear as there are no bumps in the trace. It is not a straight line due to the ESL of the trace.

Other things to try:

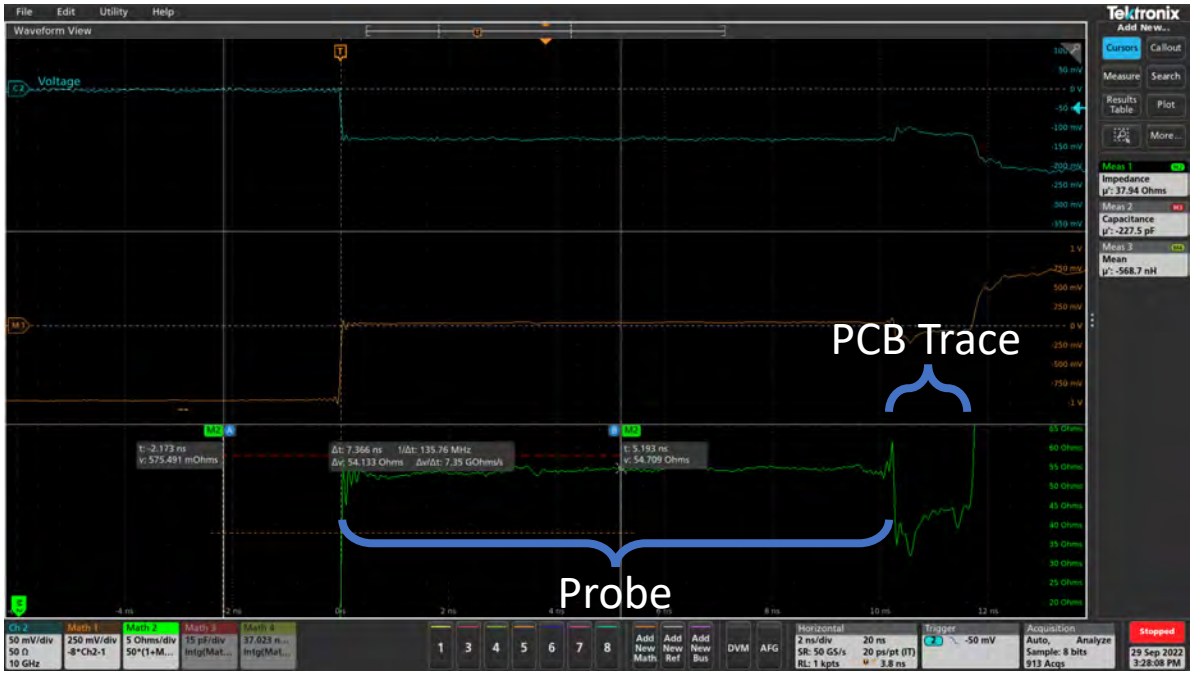
- If we can do this for cables, it should work for PCB traces. Take the probe that we attached and the TDR demo board and observe the measure the PCB traces using the TDR.



TDR Probe measurement of TP3. The trace gets wider in the middle which we can see with a change in impedance of the TDR measurement. The impedance decreases and creates a dip.

Other things to try:

- If we can do this for cables, it should work for PCB traces. Take the probe that we attached and the TDR demo board and observe the measure the PCB traces using the TDR.



TDR Probe measurement of TP5. The trace has two bumps in the trace which correspond to two dips in the TDR measurement. We can also determine the length of the trace if we know the distance between the bumps. The time it takes to go from one bump to the other bump is the reference to measure any other length of trace.

Hopefully, you know how to use the PerfectPulse® Differential TDR to measure and investigate cables and traces. The TDR is a useful measurement to determine how good the setup is and can help find the location of potential problems.

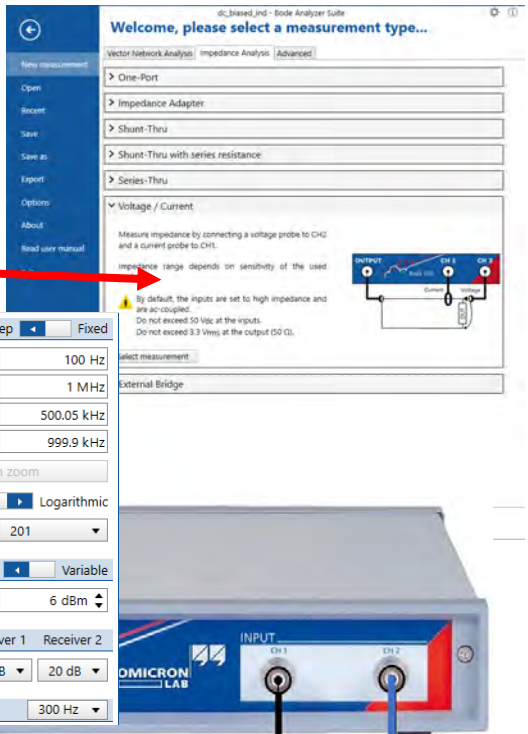
DC Biased Inductor Testing

Description:
The most important component in a switching power supply is its power inductor. A power inductor has high permeability core around which the windings are wound. It saturates when the current flowing through the conductors is larger than its saturation value. Saturation is a material property of the magnetic core. DC bias current through an inductor affects the inductance versus frequency plot. So, it is important to measure the inductance versus frequency under DC current.

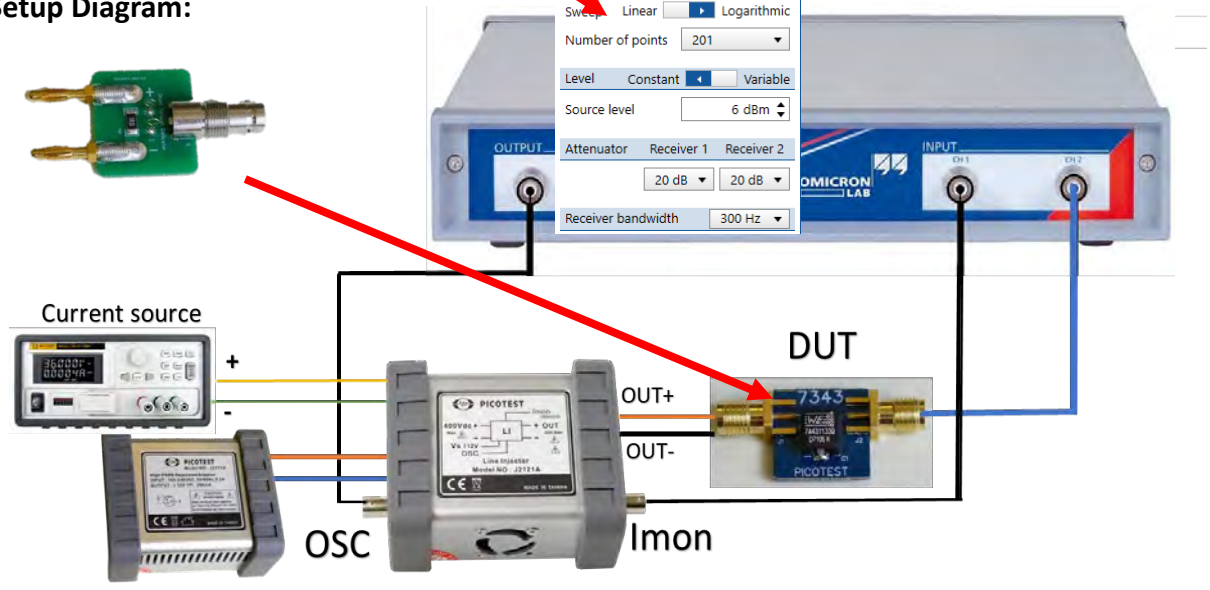
Instrument	Bode 100, P9610A/ P9611A Power Supplies
Injectors	J2121A Line Injector, J2171A High PSRR Regulated Adaptor
Probe points	N/A
Probes	N/A

Setup file: Open the setup file **dc_biased_ind.bode3**
Calibration:

1. Set the power supply for 1.5V and/or constant current limit to 750mA
2. Setup like the diagram and install the 1Ω resistor board instead of the DUT.
3. Select “Voltage/Current” in the New Measurement → Impedance Analysis menu
4. Set the source power to 6dBM and stop frequency to 1MHz or less
5. Perform a THRU calibration.



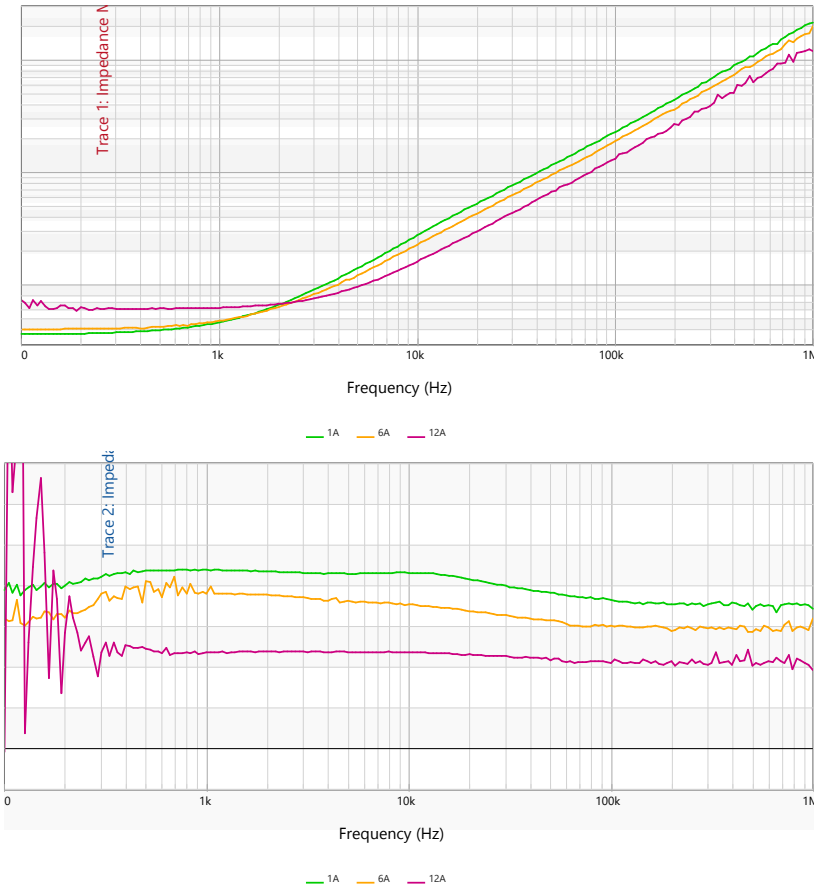
Setup Diagram:



Measurement Steps:

1. Replace the 1Ω resistor board with the DUT.
2. Set the power supply to have a constant current of 1A. This is the bias current.
3. Set Trace 1 to Magnitude.
4. Set Trace 2 to series inductance (Ls)
5. Record measurement to memory
6. Repeat for power supply at 6A and 12A.

Results:



Test results of a DC biased WE744311330, 3.3UH 6.5A inductor measured in the 2-Port shunt-through configuration using the Bode 100 VNA and J2121A. Three cases are shown. Green shows the impedance of the inductor at 1A which is 0.9 µH. Orange shows the impedance value at 6A which is like green since the inductor is rated for 6.5A. Red shows that the same inductor lost considerable inductance at 12A.

Hopefully, you know how to use the Bode100 and J2121A to measure DC biased inductors. You should also know how the bias current affects both the impedance and series inductance of an inductor. This is a measurement solution to measure inductance in 2-port shunt through method with DC current using J2121A line injector.

Additional Resources:

https://www.picotest.com/downloads/BrochureInductorBiasCurrentMeasurementsJ2121ABodeVer12Final.pdf

DC-DC Converter Input Impedance Measurement

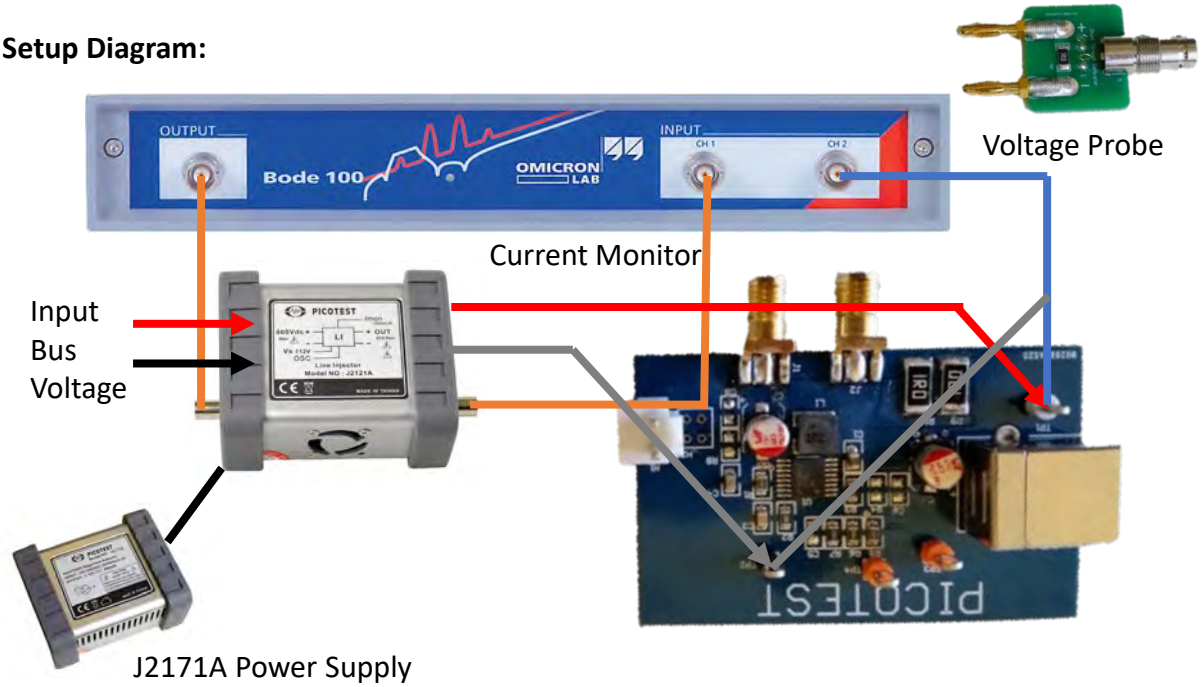
Description:
Characterizing the input impedance of a DC/DC converter is a necessary step in designing a stable input filter to counter-balance the converter's negative input resistance. The J2121A High Power Line Injector makes this challenging measurement easy. The J2121A uses the vector network analyzer's (VNA) oscillator signal to modulate the input voltage (output of the J2121A) while accommodating a wide range of voltage and current conditions. The input voltage at the converter and the input current taken from the J2121A's current sense monitor are divided in the VNA displaying input impedance. A simple through calibration corrects for the scaling of the current monitor and the probe connections.

Instrument	Bode 100, P9610A/ P9611A Power Supplies, LM20143
Injectors	J2121A Line Injector, J2171A High PSRR Regulated Adaptor
Probe points	N/A
Probes	N/A

Setup file: Open the setup file **dcdc_in_z.bode3**
Calibration:

1. Set the power supply for 1.5V and/or constant current limit to 750mA.
2. Setup like the diagram and install the 1Ω resistor board instead of the DUT.
3. Connect the Positive from the J2121A and the voltage probe to TP1.
4. Connect the Negative from the J2121A and the probe ground clip to TP2.
5. Select "Voltage/Current" in the New Measurement → Impedance Analysis menu
6. Set the source power to 6dBM and stop frequency to 1MHz or less
7. Perform a THRU calibration. Record a measurement with the Cal Board.

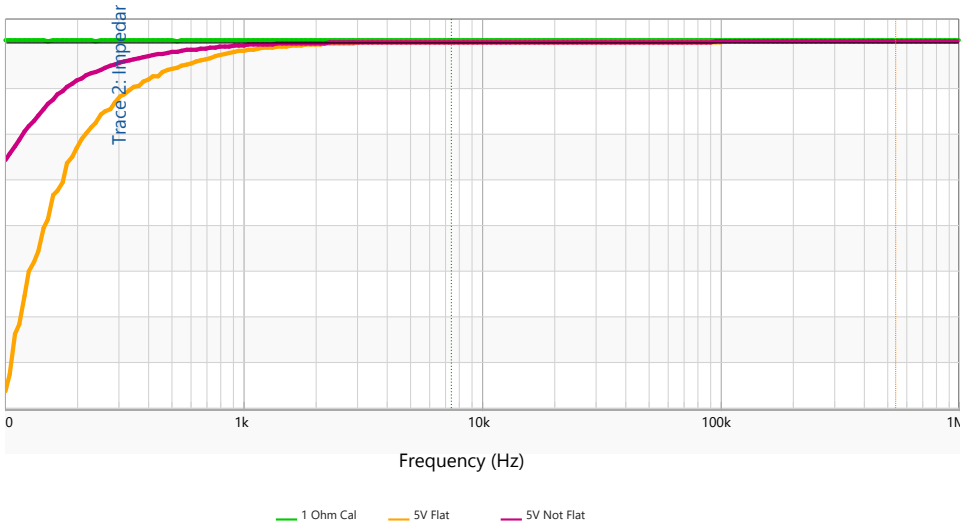
Setup Diagram:



Measurement Steps:

1. Replace the 1Ω resistor board with the LM20143.
2. Set the power supply to have a constant voltage of 5V.
3. Set Trace 1 or Trace 2 to Magnitude and Real. Turn off the other trace.
4. Record measurement to memory
5. Repeat for **Not Flat** LM20143.

Results:



A switching regulator has negative input impedance which needs to be measured to design an input electromagnetic interference (EMI) filter. The system can become unstable if the input impedance is not measured accurately during the converter design.

The negative input impedances of the LM20143 DC-DC converters are shown in the result. With a negative resistance, it can cancel out the positive resistance of the filter and cause the power to oscillate which then makes the PDN unstable. Make sure to design an appropriate filter to alleviate the issue.

Hopefully, you know how to obtain the negative input impedance of the buck converters. Obtaining this measurement is an important step in input filter design to keep the DC-DC converter stable with the filter.

Additional Resources:

https://www.picotest.com/downloads/AppNoteDCDCconverterInputImpedanceVer03Final.pdf

https://www.picotest.com/downloads/BrochureDCDCInputImpedanceMeasurementJ2121ABodeVer2Final.pdf

DC Bias Measurement for Capacitors

Description:
Every ceramic capacitor has a DC bias. This means that the capacitance will change based on what DC voltage is applied to the capacitor. In order to model the capacitor accurately, we need to know the DC bias of the capacitor. Sometimes it is provided to us by the capacitor manufacturer, but most of the time it is not. This experiment will show us how to find the DC bias points of a capacitor.

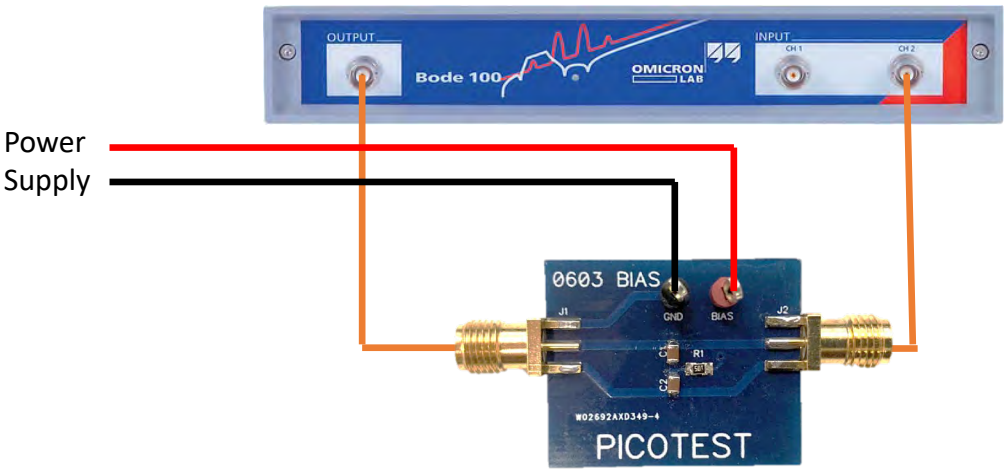
Instrument	Bode 100, P9610A/ P9611A Power Supplies
Injectors	DC Bias Capacitor Board
Probe points	N/A
Probes	N/A

Setup file: Open the setup file **dc_bias_cap.bode3**
Measurement Steps:

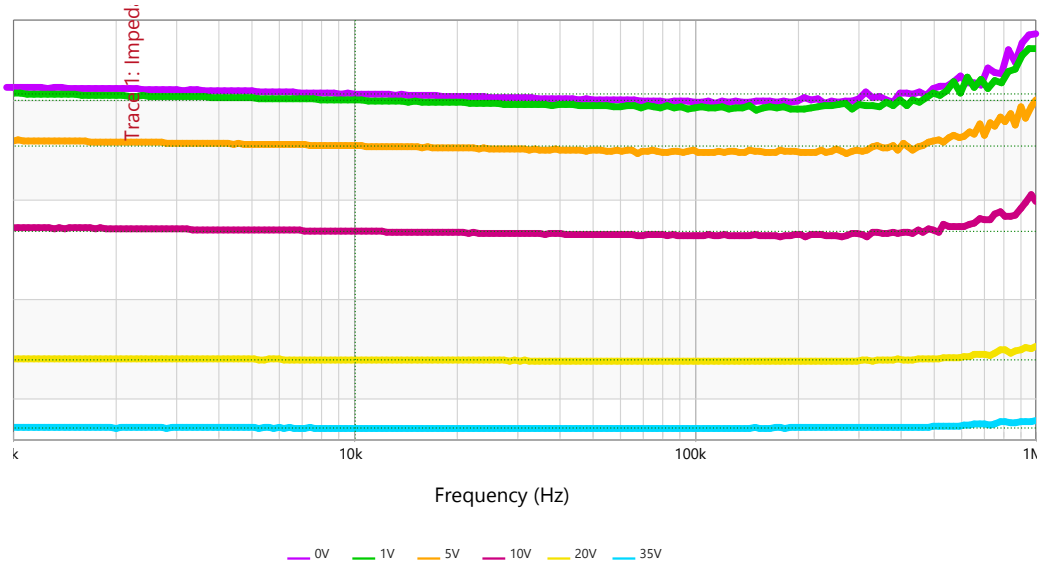
1. Setup the equipment like in the setup diagram.
2. Select a “Shunt-Thru” Measurement.
3. Replace the Bias board with a short and conduct a “Thru” calibration.
4. Change the frequency sweep from 100Hz to 100kHz.
5. Switch the Format to “Cs” to measure capacitance.
6. Make sure the power supply is off and make a measurement. This will be your nominal capacitance.
7. Change the power supply voltage to whatever DC bias points you want to test. I used 1V, 5V, 10V, 20V, and 35V.
8. Make a measurement at each DC voltage.

Note: Make sure to not exceed the voltage rating of the capacitor you are testing. I tested a 4.7uF 35V capacitor so I was able to go all the way up to 35V.

Setup Diagram:

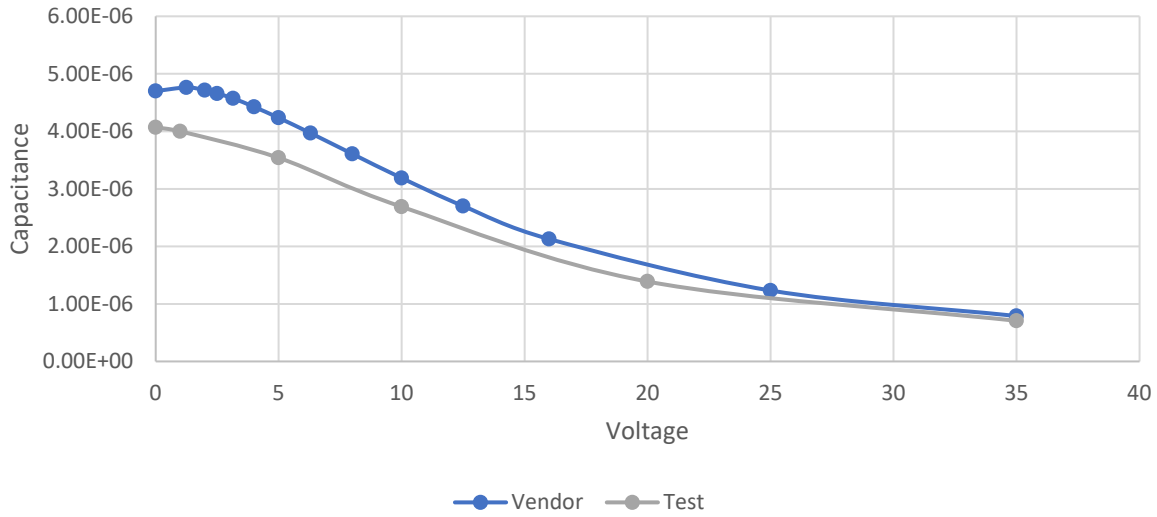


Results:



	Frequency	0V	1V	5V	10V	20V	35V
Capacitance	10 kHz	2.034 µF	2.002 µF	1.772 µF	1.343 µF	696.678 nF	354.055 nF

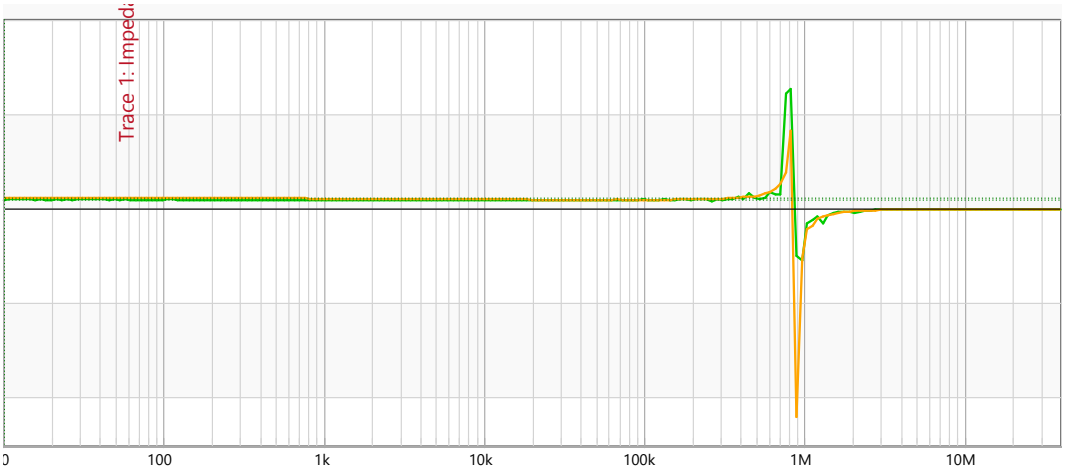
Remember the capacitance is 2X the measured value because we have two exact capacitors in series with each other. Once you have the data, copy the data files and use your favorite graphing software (I will be using Excel). Graph the points and find a curve of best fit. This will give you the DC bias equation.



Hopefully, you know how to measure the DC bias of a capacitor. This will be useful in modeling the capacitor so that you have an accurate capacitance for any DC voltage that is applied during simulation.

Other Things To Try:

- Find the AC bias of a capacitor
    - Conduct a 1-port impedance measurement.
    - Remember to calibrate the setup before taking a measurement. Conduct a SOL calibration
    - Make a measurement at +13dBm (1Vrms at 50 Ohm) and at -27dBm (10mVrms at 50 Ohms)
    - Look at a low frequency and note the capacitance difference.



	Frequency	-30dBm	13dBm
Capacitance	10 Hz	1.912 µF	2.321 µF

Remember the capacitance is 2X the measured value because we have two exact capacitors in series with each other. This difference is the AC bias. The AC bias is ~800nF.

Note: The AC amplitude will change because the impedance changes based on frequency. The source level sets a constant amplitude if it is a 50Ω load. Because the capacitor impedance changes with frequency, the amplitude is not set purely by the source level. It will be set with effect from the frequency. The amplitude will be as you set it at low frequencies but at higher frequencies, the amplitude will be attenuated.

Additional Resources:

- https://ieeexplore.ieee.org/document/9889500
- https://event.on24.com/wcc/r/3186702/ADE5E2E139D757AB1BF7A91E7DA4624A

PDN Output Impedance

Introduction:
Measuring the impedance of a device under test (DUT) is the most common and one of the most useful measurements. The impedance of power distribution networks (PDN) is useful to assess the PDN's performance and even determine the stability of the PDN without the need for the bode plots or access to the PDN's control loop. This makes the impedance measurement a crucial and important measurement for any PDN assessment.

There are two main way to measure the impedance of a PDN. The first way is using the one-port probe and conducting a one-port measurement. This way is the easiest and simplest way to measure the impedance. However, it is unable to measure low impedances. If the impedance is too low, the one-port measurement cannot accurately determine the stability and performance of the PDN. Simple is this probe's strength. It uses one cable and two pins and has a simple calibration process. It can give quick and accurate results with little setup.

The second way to measure the impedance of a PDN is through the two-port probe and making a shunt-through measurement. The two-port probe has a lower floor for impedance and thus can measure small impedances that a one-port probe would be unable to measure. The calibration process is simpler as we only need to conduct a thru calibration. However, we need extra injectors to break the DC ground loops that exist. Additionally, the impedance ceiling is much lower than its one-port counterpart but there are ways to extend it. Theoretically, it is possible to make a two-port measurement with two one-port probes but there are extra side effects that can occur like variable coupling and increased noise that need to be considered.

We will explore the Raspberry Pi and measure its output impedance with a one-port probe and assess the performance and stability of its PDN. We will showcase how to setup, calibrate, and measure the impedance of a PDN and point out things to look for in the results. At the end, you should be able to assess any PDN by measuring its output impedance.

1-Port PDN Output Impedance

Description:

Low noise depends on the level of the impedance profile. The goal is to meet the recommended voltage range of the circuit being powered under all condition and throughout the life of the product. As many circuits do not offer control loop access to assess stability, the output impedance offers a method of assessing stability as well as the PDN impedance performance. This obviates the need for a bode plot. This experiment measures the output impedance of the Raspberry Pi's voltage power rails and assesses the ripple and stability using the 1-port probe.

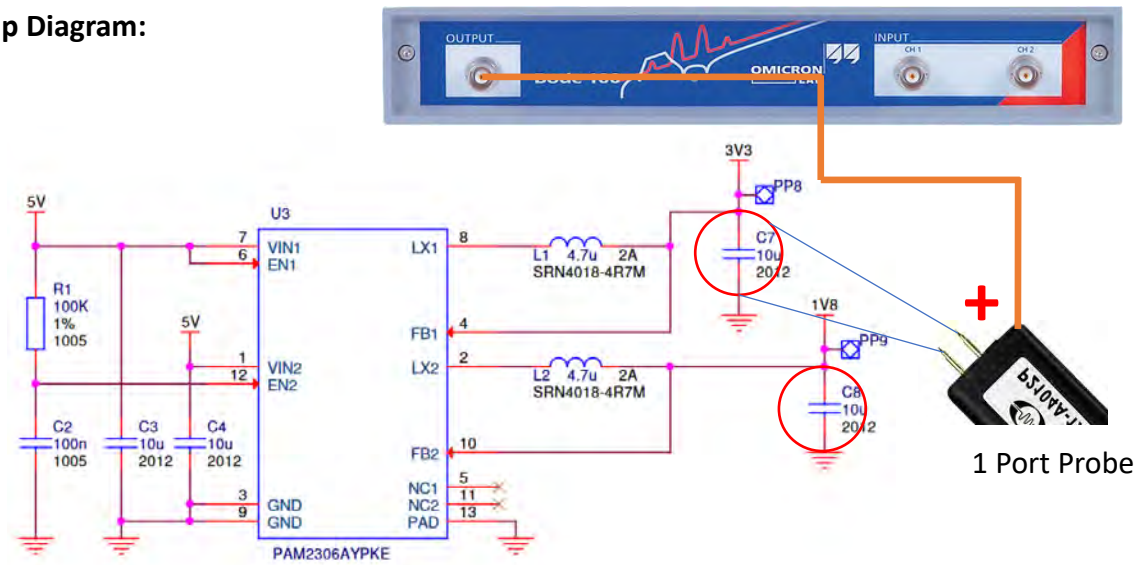
Instrument	Bode 100 VNA
Injectors	N/A
Probe point	C1, C8, and C163
Probes	1 port probe (P2104A) 100mil header

Setup:

1. Find the schematic for the Raspberry Pi Model 3 board.
2. Inside the schematic, look for the voltages that power the board especially the ones that power the processor (3V3, 1V8, VDD_CORE).
3. Then, look for any decoupling capacitors connected to those voltages.
4. Once you find some potential capacitors, go onto the Raspberry Pi board and locate the capacitors.
5. In this experiment, we located C1 for the 3V3 rail, C8 for the 1V8 rail, and C163 for the VDD_CORE rail which is a ~1.3V rail. Keep in mind that these capacitors can be hard to locate and that you want to pick ones that have easy access to them.

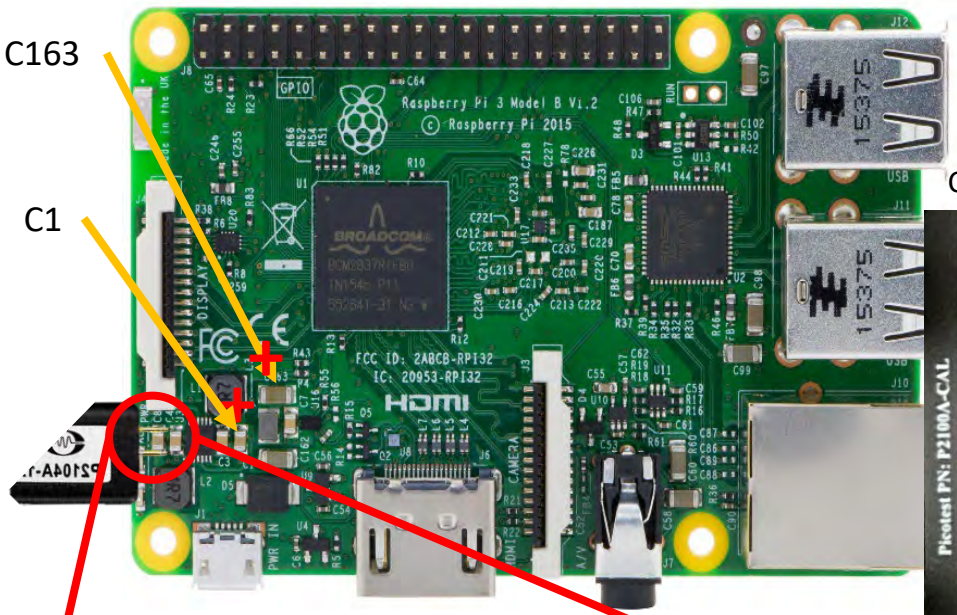
We do not need a P2130A DC Blocker because our voltages are 3.3V or lower and none of the components that are tested will be loaded by the 50Ω from the connections.

Setup Diagram:

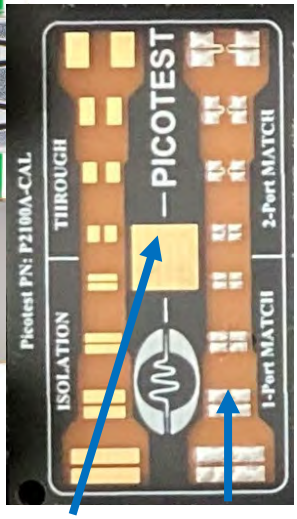


Calibration:

1. Based on the size of the capacitors, choose your probe width accordingly. For C1, C8, and C163 we will use the 100mil probe.
2. Select the “One-Port” impedance measurement.
3. Put on the probe and do calibration. Take the calibration board and run a SHORT-OPEN-LOAD (SOL) calibration.
4. Make sure to test your calibration with a known value of similar magnitude before measuring the capacitor. We usually measure a resistor of known value and verify that the output impedance is a flat line at that known value. Now the setup is ready for the first measurement.

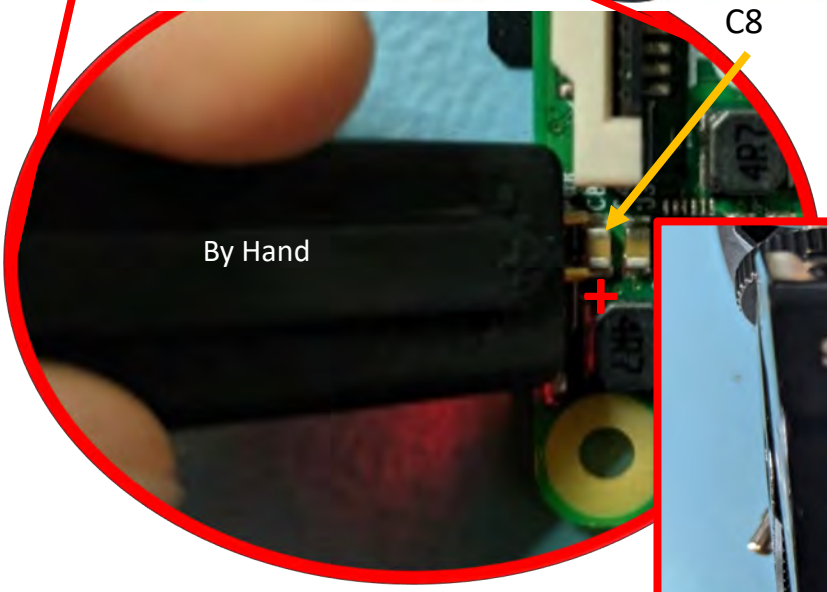


Calibration Board:



Short

Load (50Ω)



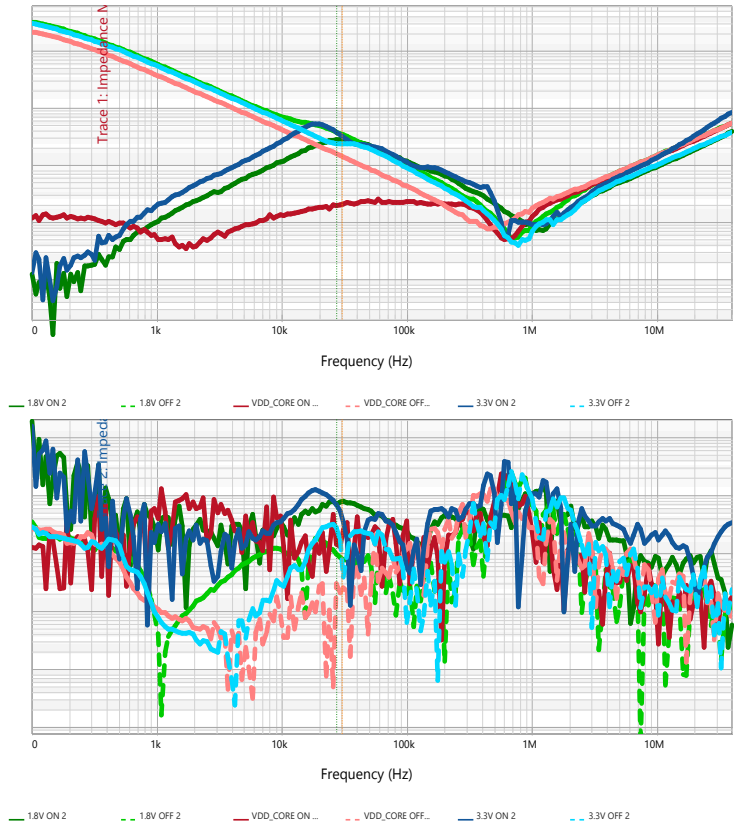
Setup file: Open the setup file **raspi.bode3**

Measurement Steps:

1. Now that everything is setup for a measurement, locate your first power capacitor.
2. Take a Digital Multimeter (DMM) and find the positive end of the capacitor.
3. Take the probe out it across the capacitor with the positive tip on the positive end of the capacitor.
4. For each capacitor, perform two measurements.
    - One in the OFF-state (board is not powered).
    - One in the ON-state (board is powered).
5. Make sure to record the measurement using the "Measurement → new memory".

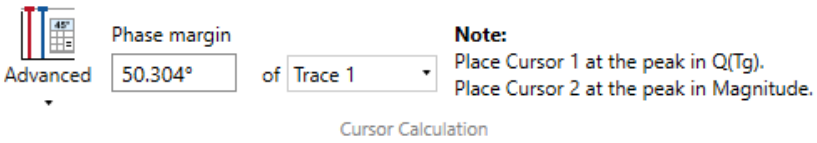
During measurement, noise will interfere make the signal unclean. Adjusting the "Source Level", "Attenuator", and "Receiver Bandwidth" can help create a cleaner and less noise signal. The "Source Level" and "Receiver Bandwidth" will be the biggest help for noise and then adjusting "Attenuator" values to prevent signal overflow.

Results:



Notice the different levels between the on state and the off state. This is because of the different DC bias across the capacitor. In the on state, we have the power rail voltage while in the off state, we have ~0V DC bias. Pay attention to the peaks in both the 1.8V and 3.3V power rails and a somewhat flat impedance for the VDD_CORE rail. We can accurately measure the phase margin and assess the 1.8V and 3.3V PDN because of the visible peaks but we will be unable to measure the phase margin of VDD_CORE due to the limitations of a one-port measurement for super small impedances to create a visible peak.

In addition, during the ON-state, select “Advanced PM Calculation” from the Cursor Basic menu. Put Cursor 1 on the peak of Q(Tg) and Cursor 2 on the peak of Impedance. Observe and record the measured phase margin.



Phase Margin Calculation for C8 (1.8V)

Thus, we need to use the two-port probe to examine the stability and impedance performance of the VDD_CORE PDN.

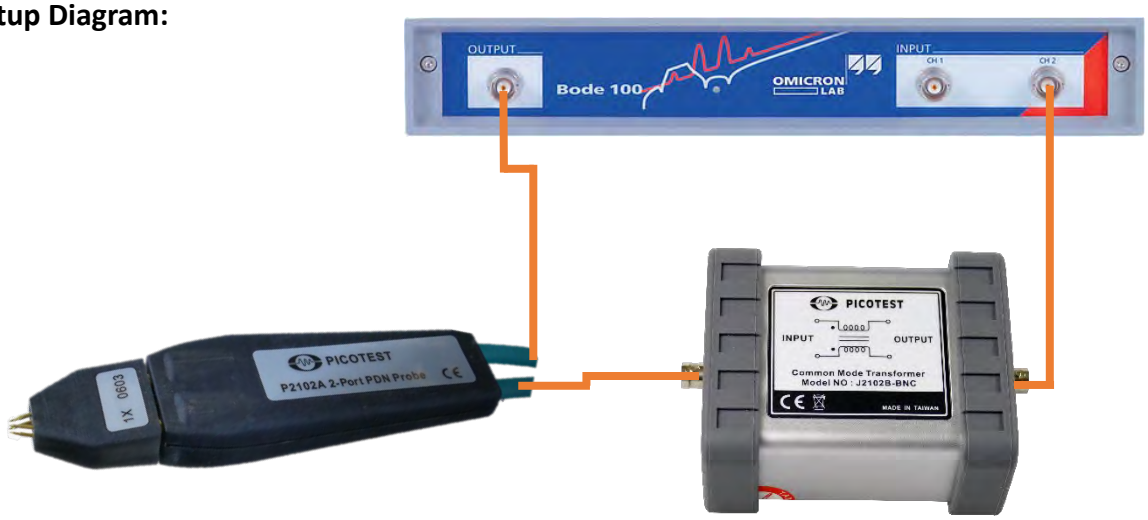
2-Port Probe PDN Output Impedance

Instrument	Bode 100 VNA
Injectors	J2102A
Probe point	C163
Probes	2-port probe (P2102A)

Setup:

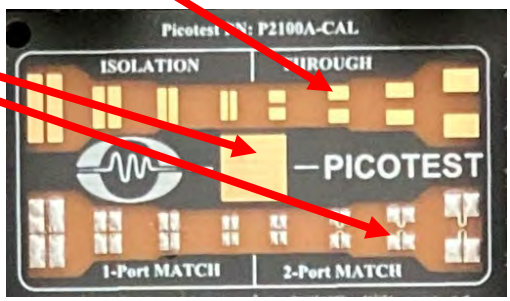
1. We will be doing a shunt thru 2-port impedance measurement.
2. Select the “Shunt-Thru” impedance measurement.
3. Connect one side of the 2-port probe to the “Output” of the Bode100.
4. Connect the other side to the “Input” of the J2102A.
5. Connect the “Output” of the J2012A to “Ch2” of the Bode100.
6. Select and attach the appropriate header for the 2-port probe. For this experiment, it will be 1206 header.

Setup Diagram:



Calibration:

1. Once everything is connected and setup, run a SOL calibration for the 2-port probe
2. Click “Full-range” or “User-range”.
3. The “Open” calibration will be a “Through” measurement.
4. The “Short” is the center pad.
5. The “Load” is the 2-port match measurement.



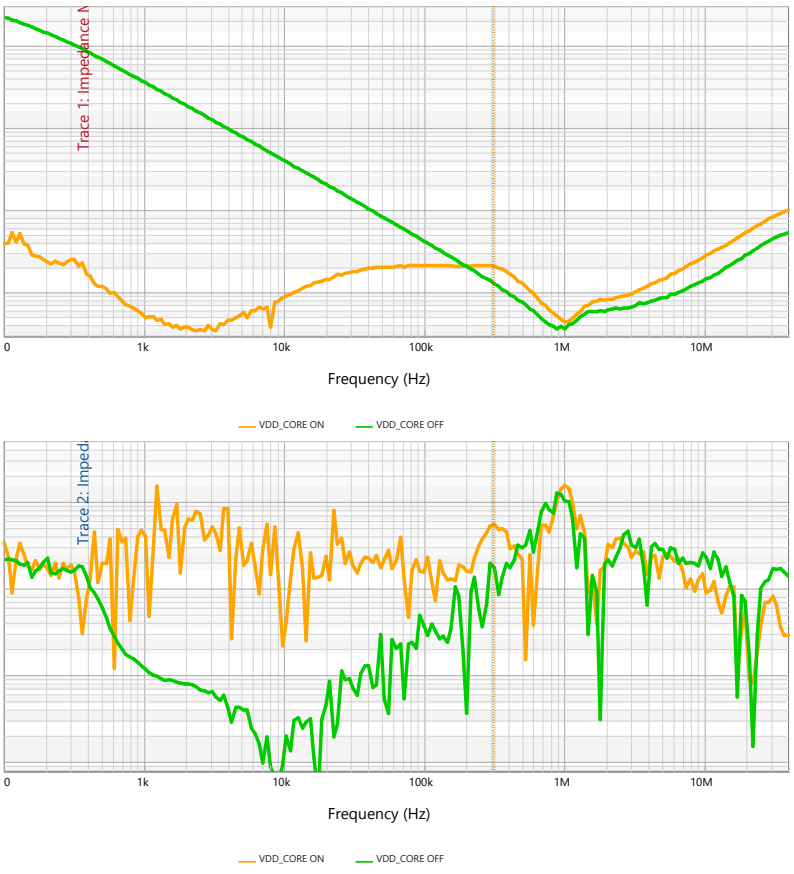
Make sure to test your calibration with a known value of similar magnitude before measuring the capacitor. We usually measure a resistor of known value and verify that the output impedance is a flat line at that known value.

Setup file: Open the setup file **raspi_two_port.bode3**

Measurement Steps:

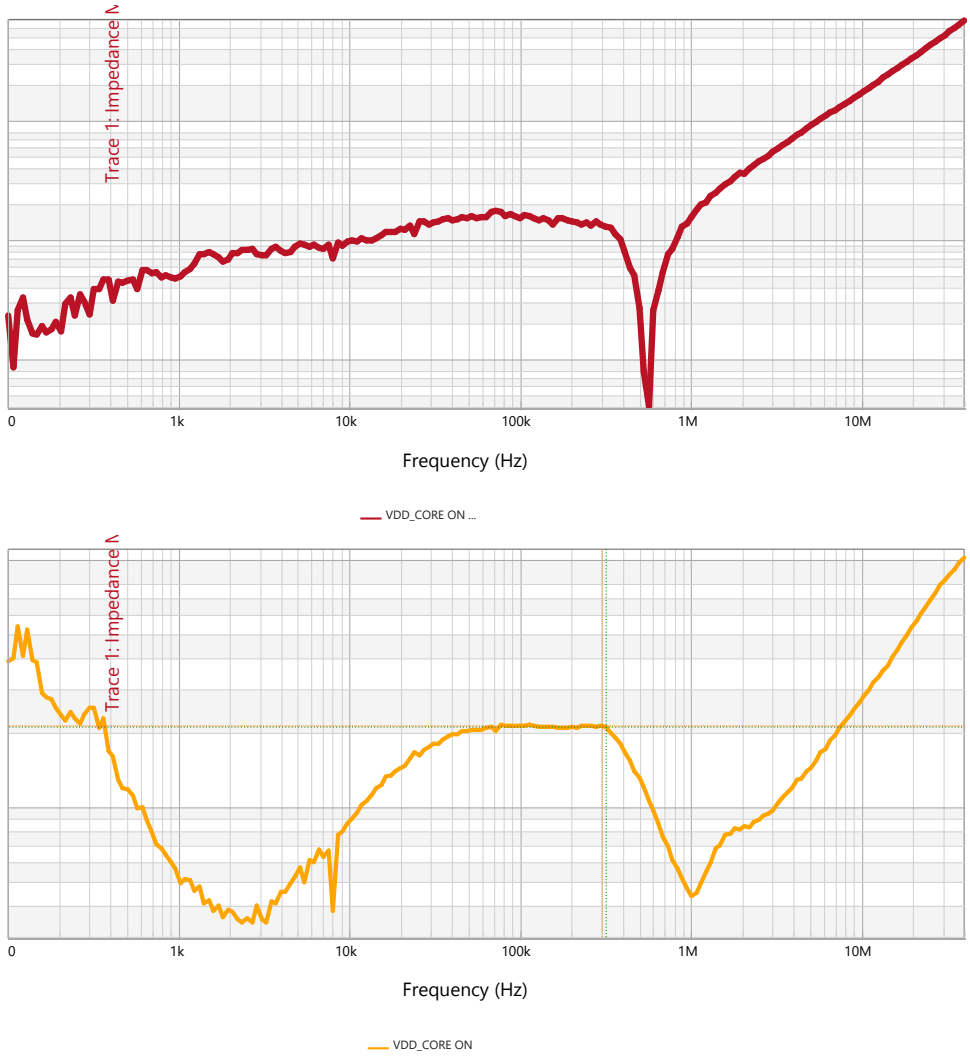
1. Use a DMM to determine the positive side of the capacitor.
2. Just like in the 1-port probe measurement, put the 2-port probe’s pins around the capacitor.
3. Make the positive end of the probe goes with the positive end of the capacitor.
4. Take an OFF-state measurement and an ON-state measurement.
5. Record the measurements to Memory.

Results:



Results:

Let us compare the 1-Port measurement to the 2-Port measurement of the VDD_CORE (C163).



The 1-Port measurement is on the top, while the 2-Port measurement is on the bottom. As we can see, the 2-Port measurement gave us something to measure the phase margin with, while the 1-Port measurement was lacking in detail. We measured the phase margin of the 2-Port, since now we can, and got a phase margin of >71°. This shows the capabilities of the 2-Port probe when the 1-Port probe is unable to conduct the measurement.

Hopefully, you now know how to measure a real life PDN with a 2-Port Probe. You can further explore the other voltage rails and continue to observe the differences between the 2-Port and 1-Port probes. Take your time with the 2-Port probe. The 2-Port measurement is not easy but offers better results than the 1-Port probe.

Appendix

VRTS3

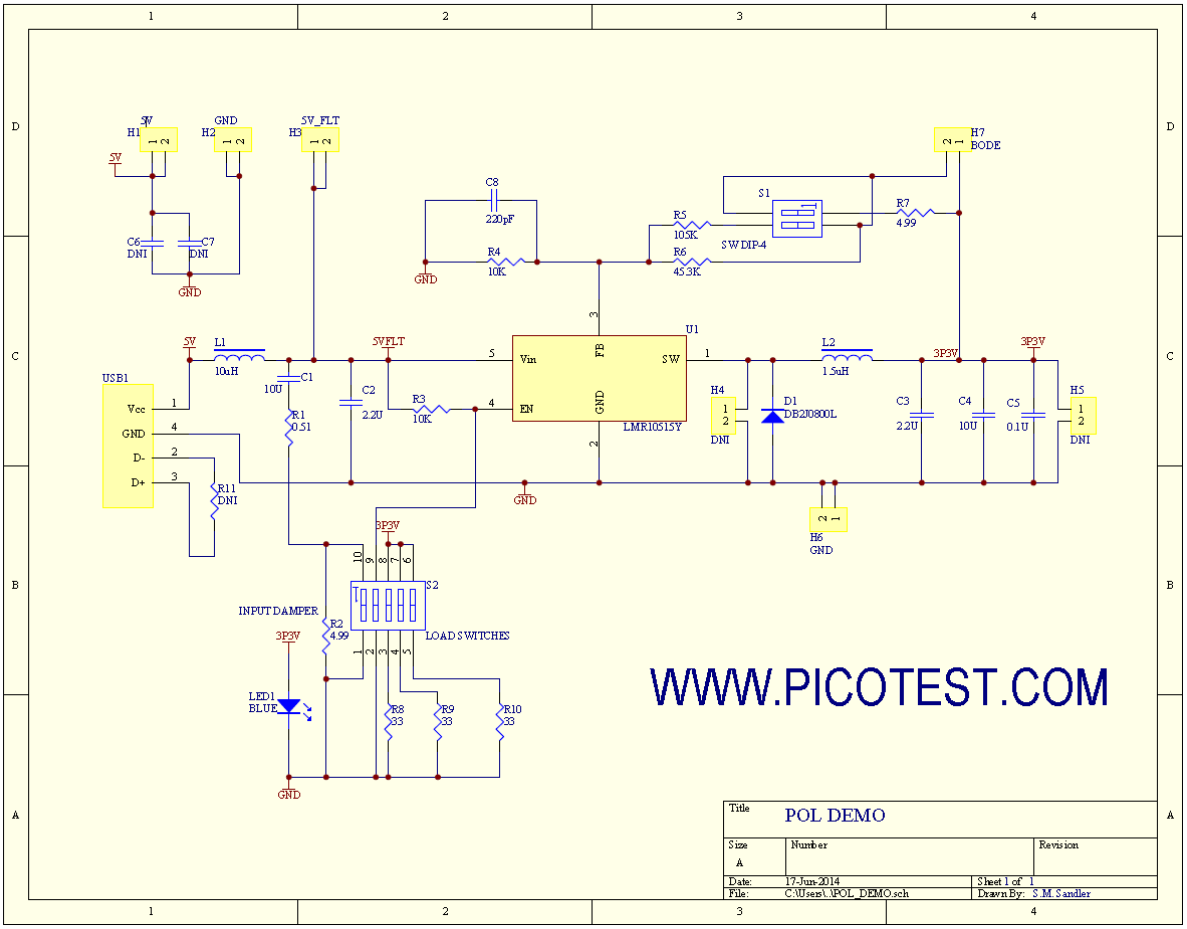
SECTION	FUNCTION
POL	5V USB input to 3.3V 2.8MHz switching regulator
REF03	2.5V low noise voltage reference
OPAMP	245MHz (Or 10MHz in some versions) bandwidth unity gain opamp buffer
LDO	LT1086 voltage regulator 5V USB input to 3.3V output
CLOCKS/BUFFERS	10MHz and 125MHz clocks
CALIBRATION	Short-Open-Load and 1 Ohm calibration ports
PLANES & CAPS	Parallel tantalum and ceramic capacitor on a small PCB plane
MICROSTRIPS	50Ω microstrips with precision aberrations - one with a ground void

POSITION	ON	OFF
	S1	
1	4.99Ω Bode plot injection resistor	Open feedback for use with the J2110A Solid State Injector
2	Sets POL output to 2.5V	Sets POL Output to 3.3V
	S2	
1	0.51Ω filter damping resistor	5.41Ω filter damping resistor
2	DISABLE POL regulator	ENABLE POL regulator
3	Add additional 100mA load to POL	
4	Add additional 100mA load to POL	
5	Add additional 100mA load to POL	
	S101	
1	0.1uF ceramic capacitor	
2	0.33uF ceramic capacitor	
	S201	
1	5.1pF NPO capacitor	
2	10pF NPO capacitor	
	S301	
1	22uF ceramic capacitor	
2	100uF 30mOhm ESR tantalum capacitor	
3	2.2uF 0.5 Ohm ESR tantalum capacitor	
4	15uF 0.4 Ohm ESR tantalum capacitor	
	S401	
1	DISABLE 125MHZ clock	ENABLE 125MHZ clock
2	DISABLE 10MHz clock	ENABLE 10MHz clock
	S402	
1	15uF tantalum damping capacitor U401	
	SEL1	

LEFT	CENTER	RIGHT
125MHz clock POL powered	125MHz clock unpowered	125MHz clock LDO powered

Shown above are the various switch positions used in the hands-on exercises. Details for the switch positions are listed as part of each exercise.

VRTS3 Schematics-POL

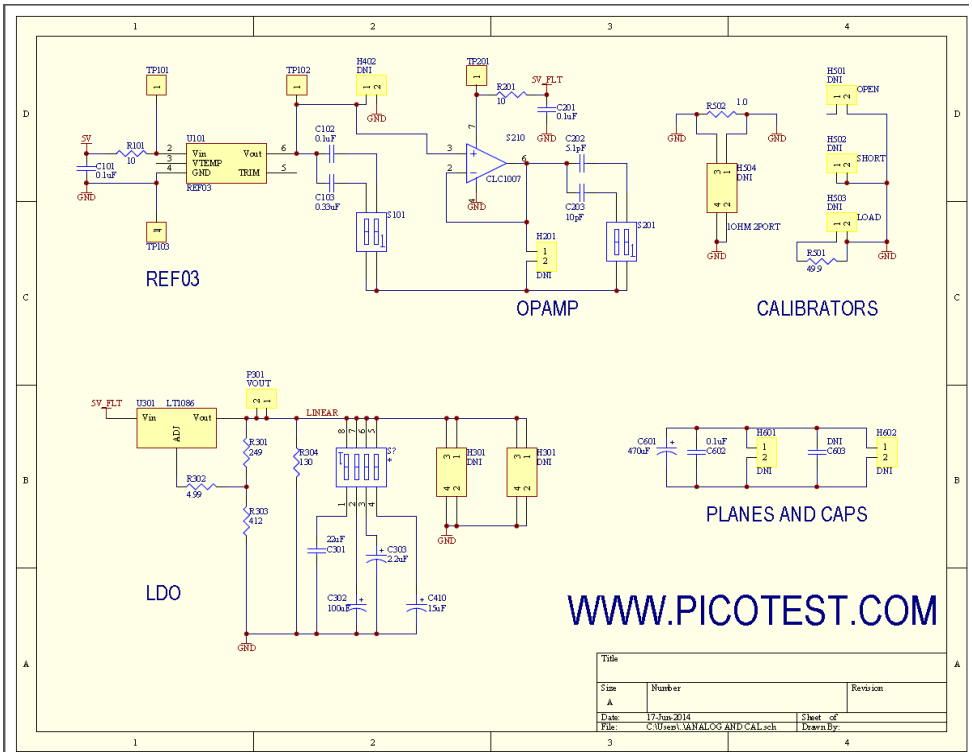


POL - 5V USB input to 3.3V 2.8MHz switching regulator

The LMR10515Y POL regulator is powered by the +5V USB input voltage. The feedback loop can be opened and closed using the top switch of S1. The bottom switch of S1 can be used to change the output voltage between 2.5V and 3.3V. There are three output resistors (R5, R6, and R7) that can be added to the output using the S2 switch to change the output current. An input damping resistor (R2) can be added at the input using the S2 switch as well.

The POL can power the clocks and buffers if the SEL1 switch is in the left position.

VRTS3 Schematics-Analog and Planes & Capacitors



Voltage Reference, Unity Gain Opamp, LDO Voltage Regulator and Planes & Capacitors

The REF03 voltage reference provides a 2.5V output voltage to the non-inverting input of the unity gain opamp. The REF03 output can be loaded with two different capacitors (C102 and C103) using the S101 switch. The capacitors are used to demonstrate the effects that output capacitance has on the stability of the REF03.

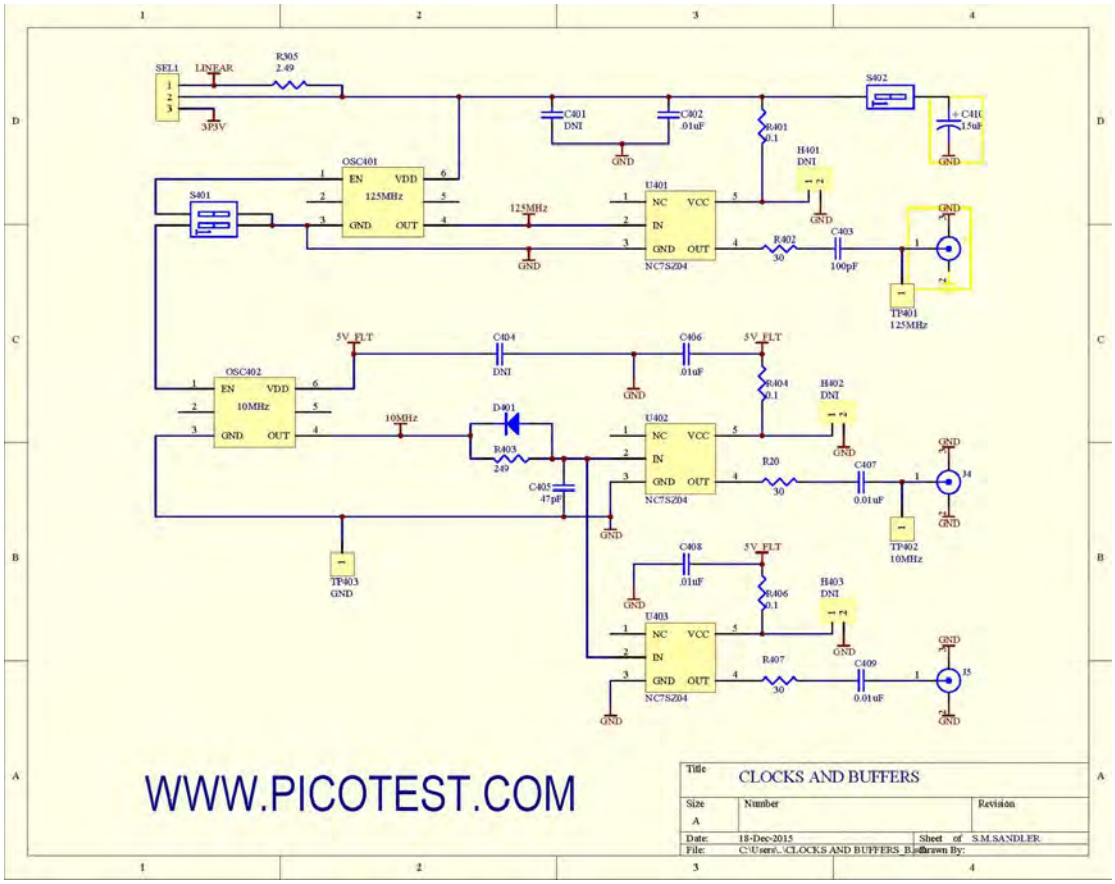
The opamp input is the 2.5V output voltage of the REF03. The opamp operates at unity gain. The opamp is powered as a single rail using the +5V input as the positive supply voltage.

The planes and caps section contains a 470uF tantalum capacitor (C601) in parallel with a 0.1uF ceramic capacitor (C602).

The LDO section includes an LT1086 that is powered by the post-filter 5V input and outputs 3.3V. The S301 switch controls which output capacitors (C301, C302, C303, and C410) are present at the load. The LDO is able to power the clocks and buffers if the SEL2 switch is in the right position.

Note : The opamp is changed to the TLC071 in some VRTS3 versions.

VRTS3 Schematics-Clocks and Buffers



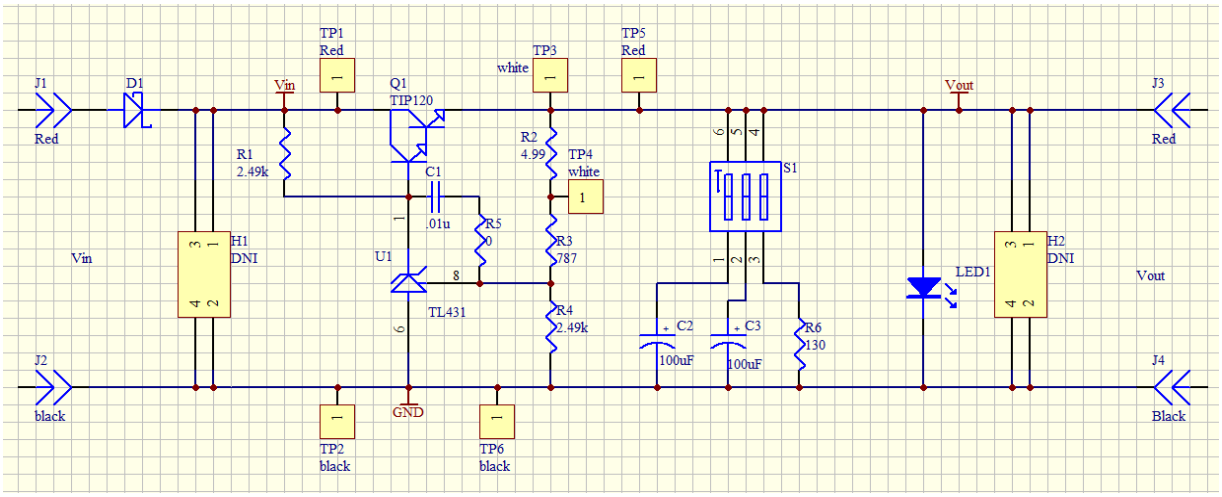
10MHz and 125MHz Clocks

The Clocks and Buffers section contains one 125MHz clock and two 10MHz clocks, along with buffers for each clock.

The 125MHz clock output is connected to one NC7SZ04 inverter (U401). The 10MHz clock output is connected to two NC7SZ04 inverters (U402, U403) in parallel.

A 15uF damping capacitor (C410) can be connected to U401 by using the S402 switch. An EMI probe can be used to observe the various frequencies of the clocks.

VRTS1P5 Schematic



The circuit is a discrete BJT voltage regulator with a 7-10V input and a 3.3V output. The BJT is controlled by a TL431 shunt regulator. C1 and R5 provide frequency compensation, R2 is the injection transformer terminating resistor and R3 and R4 are the output voltage sense divider. Two different output capacitors can be selected using S1-1 and S1-2. One capacitor, an aluminum electrolytic provides excellent phase margin while the other results in approximately 40 degrees of phase margin. A blue LED is powered by the output, providing a visual indication of power on and also a load of approximately 20mA. An additional 25mA of load current can be switched on or off using S1-3.

The input voltage range is 7-10V (compatible with the Picotest wall adapter power supply, R1 changed to 499Ω) and the output voltage is fixed at 3.3V with a 100mA maximum output current.

- TP1 - Input voltage meter or probe
- TP2 - Ground for meter or probe
- TP3 - Bode injection
- TP4 - Bode injection
- TP5 - Output voltage meter or probe
- TP6 - Ground for meter or probe

S1-1, C2 - Aluminum capacitor, excellent phase margin – too high for Non-invasive measurement (NISM)
S1-2, C3 - Tantalum capacitor, poor phase margin – ~40deg can be measured with NISM
S1-3, R6 - 130Ω load resistor for an additional 25mA load

The VRTS1.5 supports PSRR, reverse transfer, transient load step, Bode plot, non-invasive stability measurement (NISM), and noise density tests.