UBM

Evaluation of Gallium Nitride HEMTs for VRM Designs

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SPEAKERS

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Venkatesh Avula is pursuing graduate study and research at the University of Idaho. He has 10 years of experience in signal integrity, power delivery analysis, and characterization of PCB, package and on-chip interconnects at various companies, including Seagate (formerly Avago/LSI) and Tektronix.

Steve Sandler

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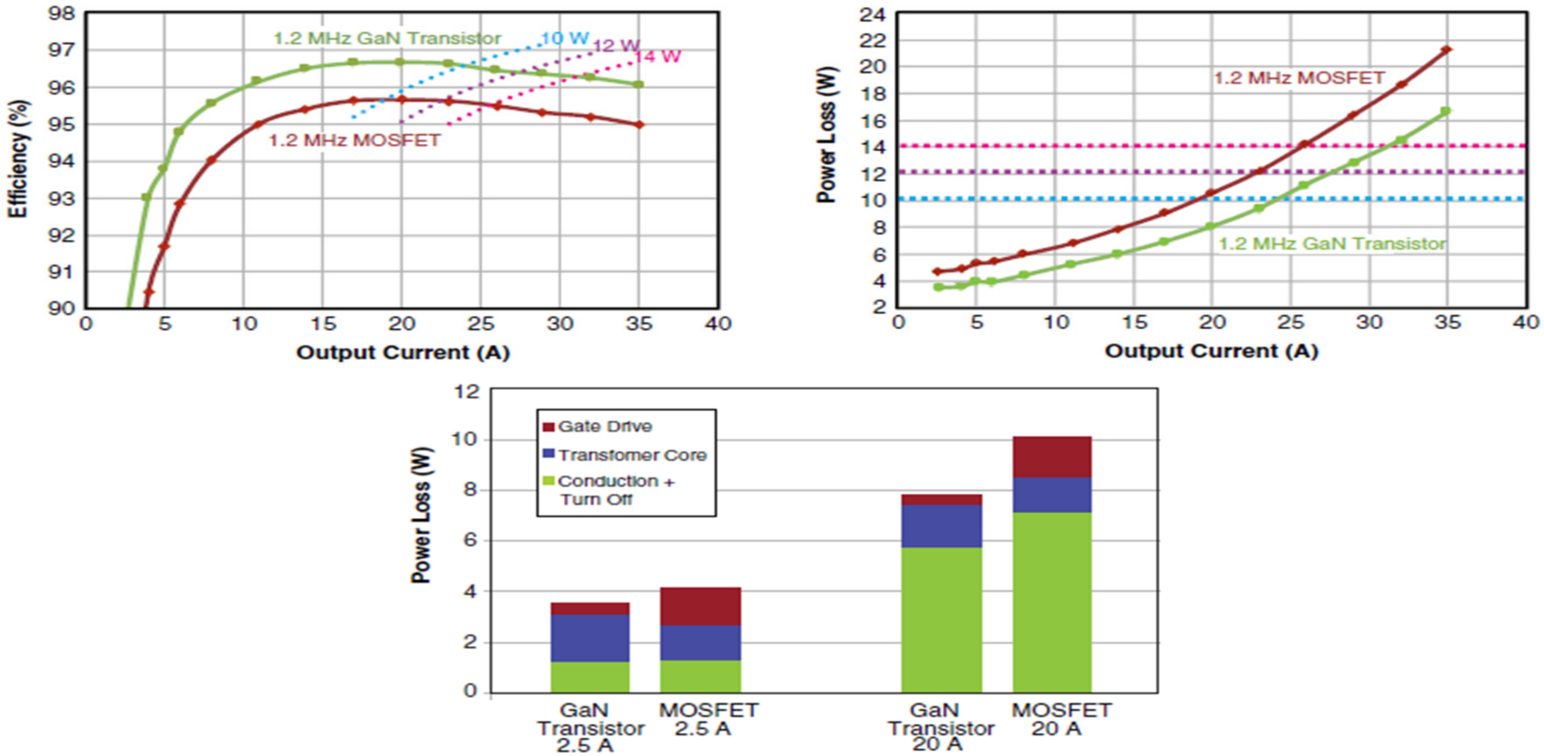
Steve Sandler has more than 35 years' experience in the design, analysis, and troubleshooting of power conversion and system level equipment for commercial, military, and space applications. Steve is the CEO of Picotest.com, a company that designs and distributes test equipment accessories designed for test and troubleshooting power systems. Steve is also the founder and chief engineer of AEi Systems, a leading analysis and modeling company specializing in worst case analysis of high reliability systems. Steve has authored several books related to power electronics including most recently the book entitled "Power Integrity - Measuring, Optimizing and Troubleshooting Power Systems."

Evaluation of Gallium Nitride HEMTs for VRM Designs



Example-48V to 12V bus converters operating at a switching frequency of 1.2MHz

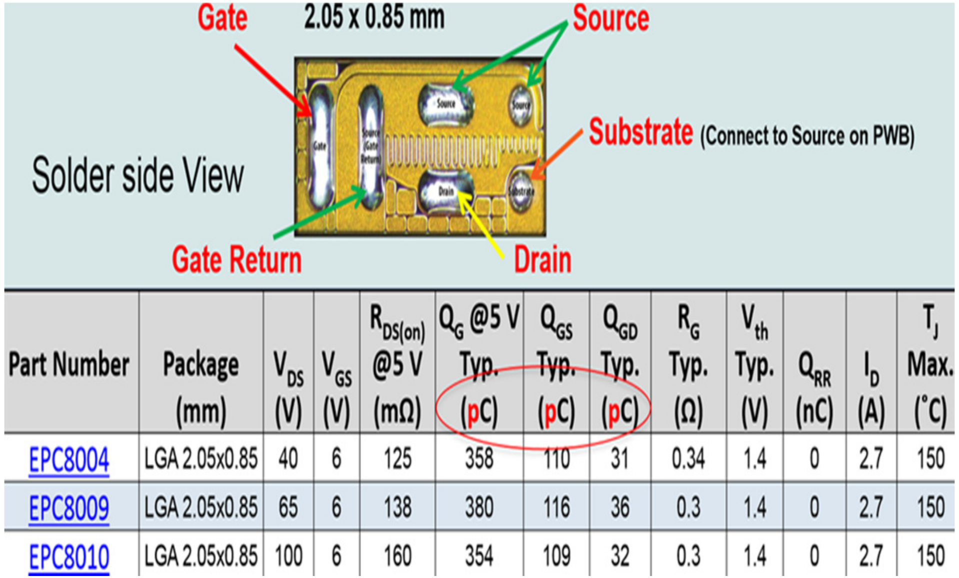
Outline

- **Challenges in VRM design:**
  - Power delivery performance
  - Cost and space

- **Can eGaN solve these challenges?**
  - Material properties
  - Electrical properties

- **Incremental adoption of GaN**
  - Migrating a linear regulator design
  - Migrating a switching regulator design

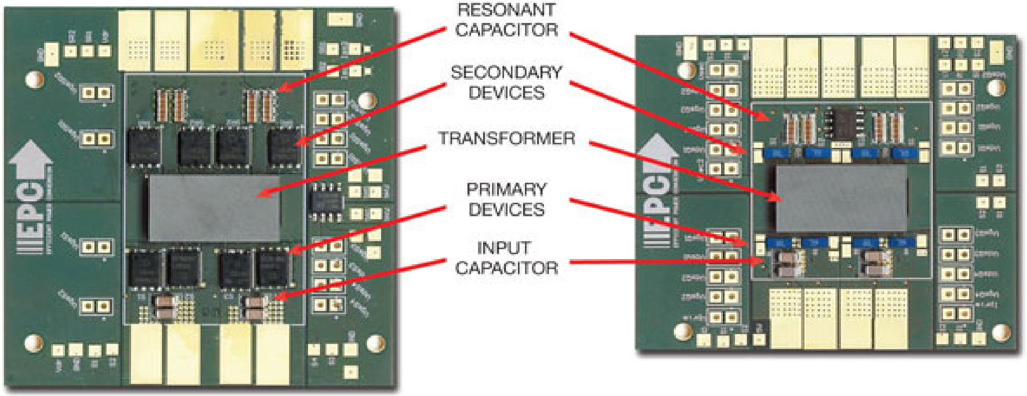
- **Conclusion**



Part Number	Package (mm)	V_{DS} (V)	V_{GS} (V)	$R_{DS(on)}$ @5 V (mΩ)	Q_G @5 V Typ. (pC)	Q_{GS} Typ. (pC)	Q_{GD} Typ. (pC)	R_G Typ. (Ω)	V_{th} Typ. (V)	Q_{RR} (nC)	I_D (A)	T_J Max. (˚C)
EPC8004	LGA 2.05x0.85	40	6	125	358	110	31	0.34	1.4	0	2.7	150
EPC8009	LGA 2.05x0.85	65	6	138	380	116	36	0.3	1.4	0	2.7	150
EPC8010	LGA 2.05x0.85	100	6	160	354	109	32	0.3	1.4	0	2.7	150

Challenges in VRM design

- **Need of the hour: squeeze more and more features into less board space**
  - eGaN offers to solve this conundrum of cost and space.
  - Example-48V to 12V bus converters operating at a switching frequency of 1.2MHz

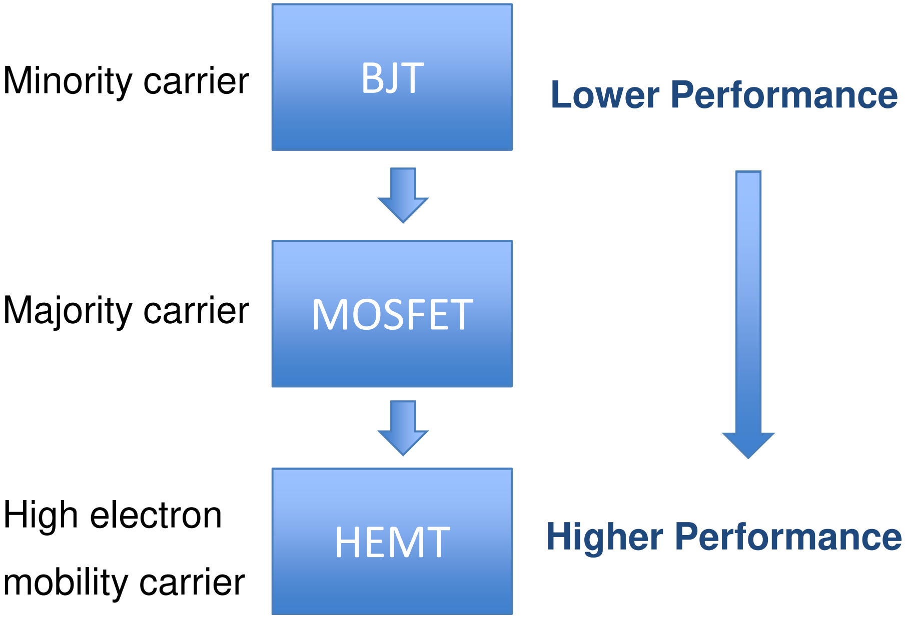


(a) Si MOSFET

(b) GaN HEMT

- **For existing Si FET based VRM designs, can we improve by supplanting with eGaN?**

Evolution of Transistor devices



Minority carrier

BJT

Lower Performance

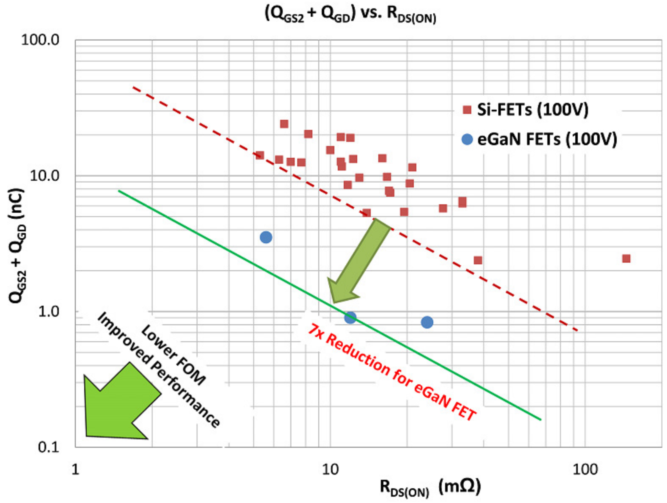
Majority carrier

MOSFET

High electron mobility carrier

HEMT

Higher Performance



Switching - Figure of merit

GaN vis-a-vis Silicon FET: material properties

Parameter	Silicon	GaN
Band Gap E_g (eV)	1.12	3.39
Critical Field E_{crit} (MV/cm)	0.23	3.3
Electron Mobility μ_n ($cm^2/V.s$)	1400	1500
Permittivity ε_r (F/m)	11.8	9

- **Higher band gap:**
  - Results in lower leakage current.
  - Allows higher temperature operating capability.
- **Higher Critical field:**
  - Results in higher drain-source breakdown voltage.
- **Higher mobility:**
  - Results in lower Rds-on resistance, thereby lower conduction losses during power conversion.

GaN vis-a-vis Silicon FET: electrical properties

- **Lower Rds-on:**
  - Lower conduction loss, higher conversion efficiency.
- **Lower leakage current:**
  - Lower leakage losses.
- **Lower capacitance:**
  - Allows faster switching speed.
  - Also lower gate charge required to turn on.
- **Lower Gate drive voltage margin:**
  - 1V margin for eGaN – a tight requirement.
- **Packaging:**
  - Much smaller.
- **Radiation tolerance:**
  - Inherently more radiation tolerant.

Parameter	Silicon MOSFET (Infineon BSC060N10NS3G)	eGaN HEMT (EPC2001)
Leakage current	1000 µA	300 µA
On-resistance	6.6 mΩ	5.6 mΩ
Capacitance	3700 pF	850 pF
Gate Charge Q_G	51 nC	8 nC
Diode forward voltage, V_{SD}	0.8V	1.75V
Reverse recovery charge Q_{rr}	6.4 µC	54 nC
Reverse recovery time t_{rr}	630 ns	30 ns
Transconductance G_{fs}	85 S	100 S
Source-Drain Forward Voltage, V_{SD}	1 V	1.75 V
Threshold voltage change over temperature 25^0 to 125^0	38% decrease	3% increase
Maximum Switching speed	<1MHz	100s of MHz
Package size	6.3 x 5.0 mm	4.1 x 1.6 mm

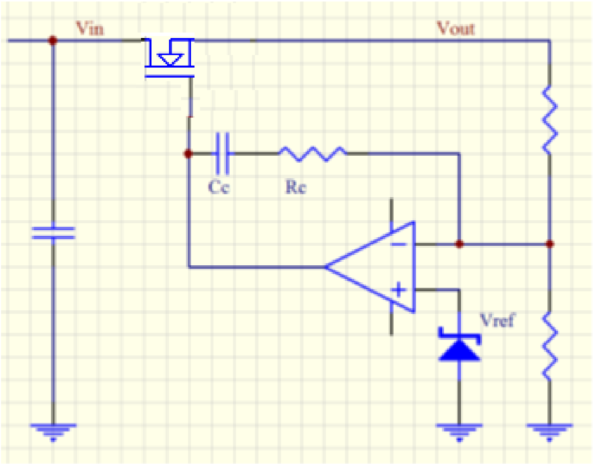
Linear regulators: figures of merit

- **Linear regulators:**
  - primarily used in applications, at lower operating current levels.
  - or those applications where voltage rail noise must be kept to a minimum.
- **Significant figures of merit:**
  - output impedance
  - dropout voltage (headroom)
  - PSRR

Regulator FOM	Key Pass Device Parameters	Si MOSFET	eGaN HEMT	Winner
Output Impedance	Transconductance	Lower	Higher	eGaN
Dropout Voltage	R_{DSon}	Higher	Lower	eGaN
PSRR	Junction Capacitance	Higher	Lower	eGaN
Noise	Junction Noise	Higher	Lower	eGaN
Physical Size	Electron Mobility	Lower	Higher	eGaN
	Breakdown Field	Lower	Higher	eGaN
Radiation Tolerance	Radiation Hardening	Not Hard	Hard	eGaN
Junction Temperature	R_{theta}	Lower	Higher	Si

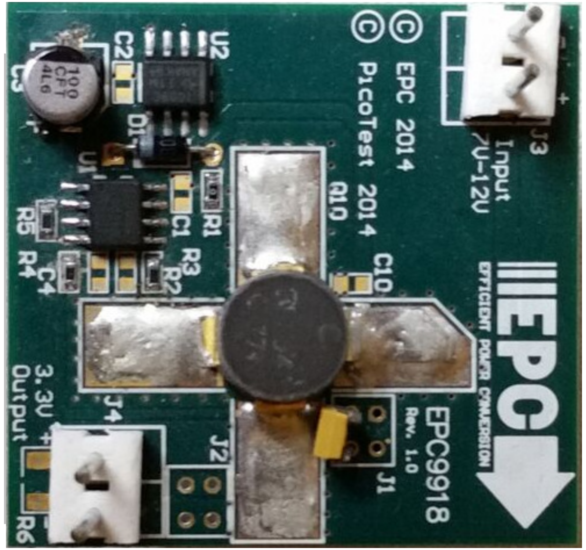
Linear regulators: migration path

- **The migration path is simple with few concerns:**
  - The gate source voltage must be kept below 5V or the eGaN HEMT device can be damaged.
  - Only N-channel designs can be migrated as there are no P-channel eGaN HEMT devices.
  - Sufficient cooling to account for the higher thermal resistance resulting from the smaller size of the eGaN HEMT device.



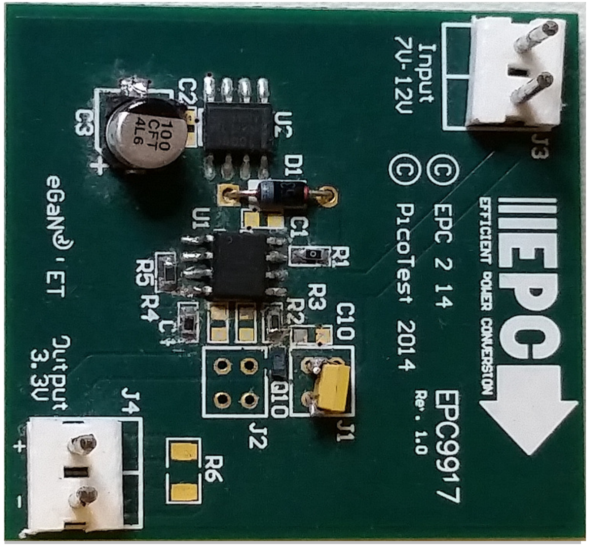
Linear regulators: migration path example

Si FET based



VS.

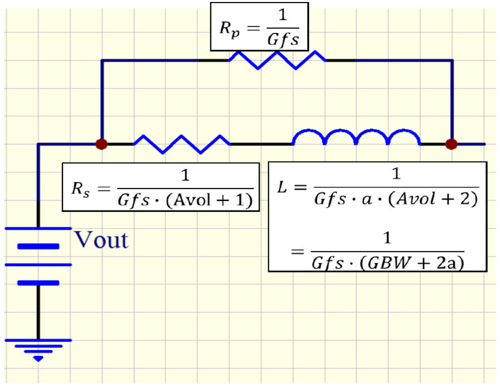
eGaN based



- **Smaller design:** Space saver

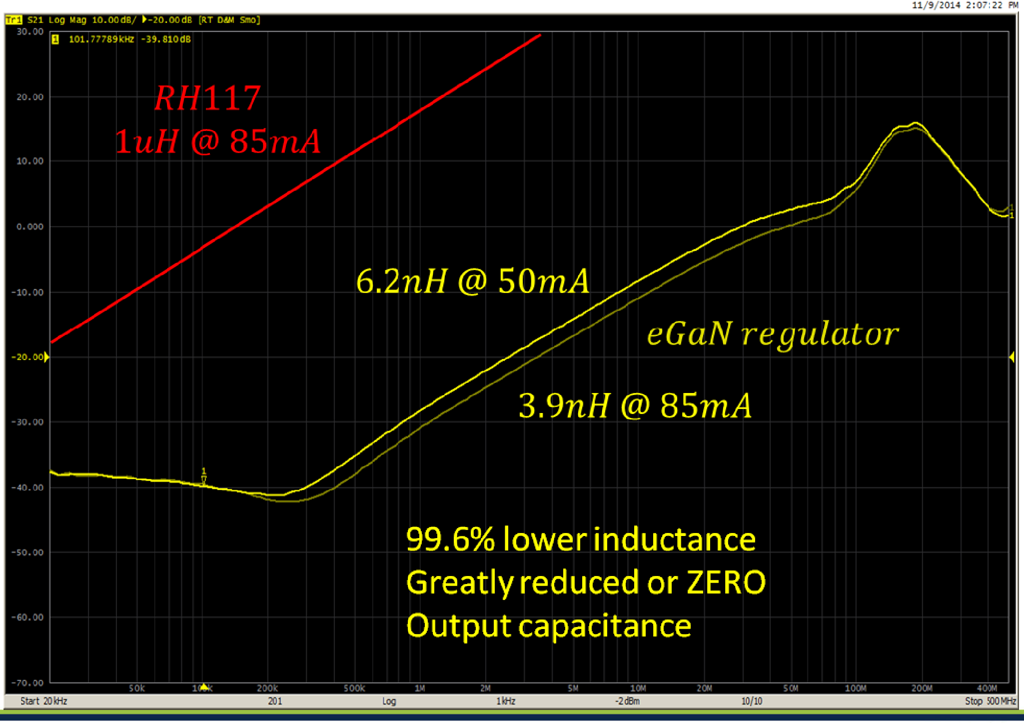
Linear regulators: output impedance

- **Regulator impedance depends on pass transistor's transconductance and loop gain:**
  - Transistor device's dynamic junction resistance, $R_j = \frac{NKT_k}{q\,I_{out}} = \frac{26mV}{I_{out}}N = 1/G\,fs$
  - Loop gain, as a dominant pole and open loop DC gain, $T = \frac{a\,Avol}{s+a}$
  - Regulator impedance, $Zreg = R_j\frac{1}{(1+T)} = \frac{1}{Gfs}\frac{1}{(1+T)} = \frac{1}{Gfs}\frac{1}{\left(1+\frac{a\,Avol}{s+a}\right)} = \frac{(s+a)}{Gfs\,.\,a.\,(Avol+1)+s}$
  - Output impedance, can be obtained by differentiating the regulator impedance, $Z_{reg-AC} = \frac{\partial}{\partial s}\left[\frac{(s+a)}{Gfs\,.\,a.\,(Avol+1)+s}\right] = \frac{1}{Gfs\,.\,a.\,(G+1)+s} - \frac{(s+a)}{Gfs\,.(a.\,(G+1)+s)^2}$
  - Since the transconductance of eGaN is much higher, linear regulator impedance is decreased by replacing Si with eGaN.



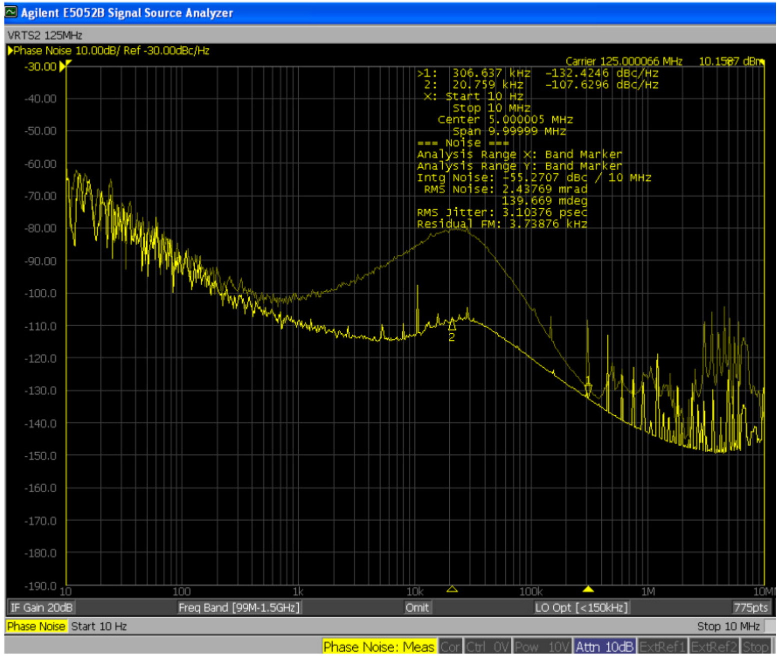
Linear regulators: output impedance

Comparison of measured output impedance benefit from higher bandwidth Si three terminal regulator (Red trace) vs eGaN (yellow traces)



99.6% lower inductance
Greatly reduced or ZERO
Output capacitance

Linear regulators: output impedance



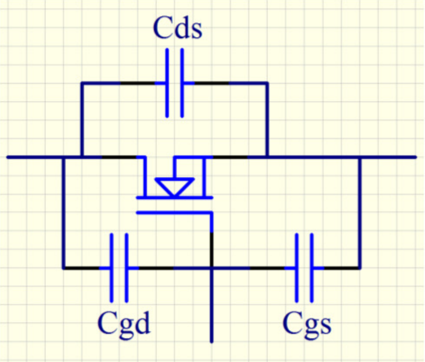
```
Phase Noise 10.00dB/ Ref -30.00dBc/Hz
                                       Carrier 125.000066 MHz    10.1587 dBm
>1:  306.637 kHz  -132.4246 dBc/Hz
 2:  20.759 kHz   -107.6296 dBc/Hz
 X: Start 10 Hz
      Stop 10 MHz
    Center 5.000005 MHz
      Span 9.99999 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -55.2707 dBc / 10 MHz
 RMS Noise: 2.43769 mrad
              139.669 mdeg
RMS Jitter: 3.10376 psec
Residual FM: 3.73876 kHz
IF Gain 20dB    Freq Band [99M-1.5GHz]    Omit    LO Opt [<150kHz]    775pts
Start 10 Hz                                                    Stop 10 MHz
```

Comparison of measured phase noise of clock powered by linear regulators, Si LM317 (dim memory trace) vs eGaN (bright data trace)

Linear regulators: Dropout voltage and PSRR

- **Dropout voltage**
  - It is the minimum voltage drop across the regulator as it delivers the load current : $V_{dropout} = I_{out}\, RDS_{on}$
  - As eGaN offers lower RDSon, the dropout voltage performance is improved with replacement of Si MOSFET device by eGaN.

- **Power supply ripple rejection ratio (PSRR)**
  - AC voltage fluctuations presented at the input to a regulator result in corresponding noise at the output, $PSRR = \frac{\Delta V_{out}}{\Delta V_{in}}$
  - PSRR is a measure of the ability to reject such input variations.
  - Since eGaN HEMT offers significantly reduced junction capacitance compared to Si MOSFET, the PSRR performance is directly improved.



Transistor's equivalent capacitance model

Switching regulators: figures of merit

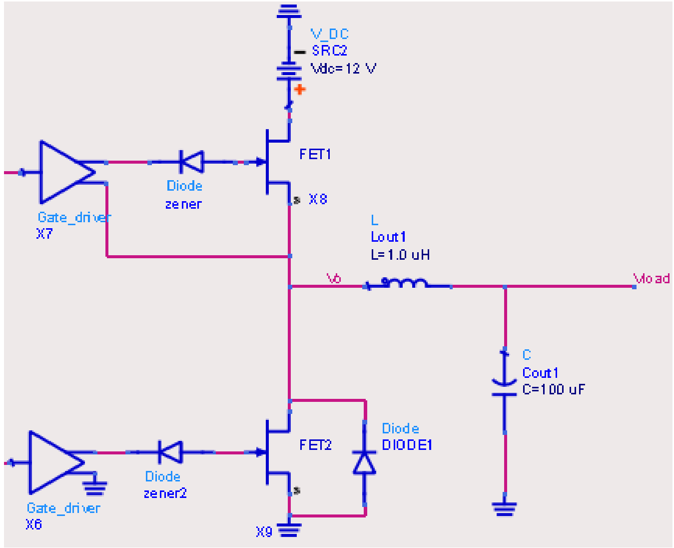
- **Switching regulators:**
    - Primarily for those at higher operating current levels or where efficiency is paramount.
    - And where there is high voltage difference between input and output.
- **Significant figures of merit:**
    - Efficiency
    - Physical size
    - Switch node waveforms
    - EMI

Regulator FOM	Key Switch Device Parameters	Si MOSFET	eGaN HEMT	Winner
Efficiency	RDSon,	Higher	Lower	eGaN
	Reverse conducting body diode drop,	Lower	Higher	Si
	Package inductance,	Higher	Lower	eGaN
	capacitance	Higher	Lower	eGaN
Gate drive voltage overshoot tolerance	Gate drive voltage margin	Higher	Lower	Si
Layout parasitic impact on performance	Gate drive voltage margins	Higher	Lower	Si
Temperature range	Temperature coefficient of RDSon and Vth	Higher	Lower	eGaN
Switch node waveform	Electron Mobility,	Lower	Higher	eGaN
	Gate charge	Higher	Lower	eGaN
Switching frequency	Gate charge,	Higher	Lower	eGaN
	Device capacitance	Higher	Lower	eGaN
Size	Package, need for external components	Bigger	Smaller	eGaN

Switching regulators: migration path

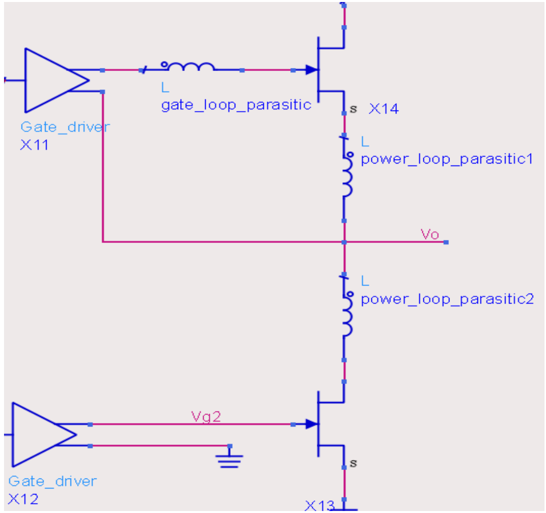
- **Migration is not trivial - several concerns**
  - If dead time is excessive,
  - Add Schottky diode.
  - Configure the gate controller to have lease possible dead time.
  - Lesser the dead time, lesser the reversion conduction flow and higher the power conversion efficiency

  - If gate controllers have high gate drive voltage, as most do,
  - The gate-source voltage must be kept below 5V, or the eGaN HEMT device will be damaged.
  - Add reverse biased Zener diode to shift gate level to 5V

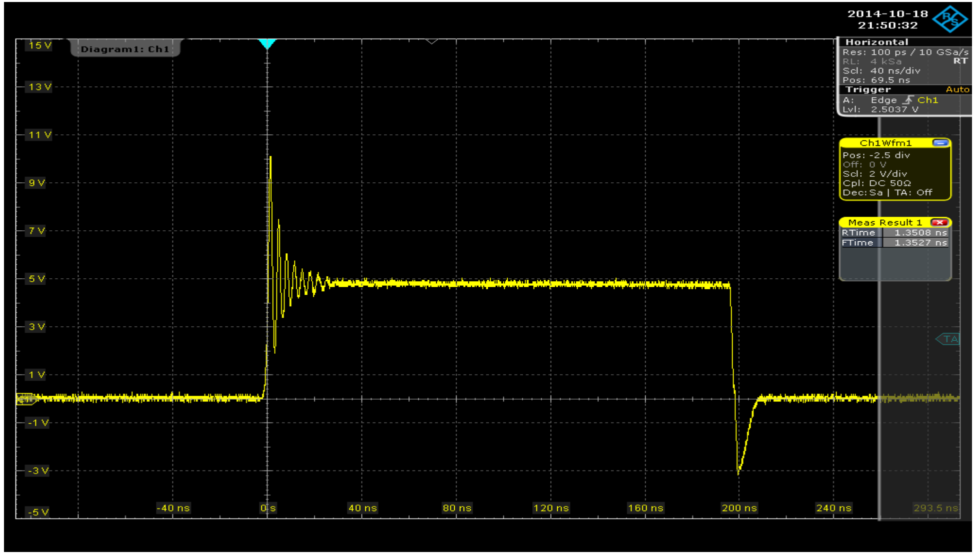


Switching regulators: migration path

- **eGaN HEMT is susceptible to board layout parasitics**
  - eGaN HEMT is vulnerable to Ldi/dt and Cdv/dt spikes, as it runs at higher di/dt and dv/dt rates.
  - Such overshoots at the gate drive can exceed the recommended 6V of eGaN HEMT, potentially damaging the device.
  - Also, overshoot voltages incur power loss.
  - Therefore, the PCB board layout needs to be optimized for suitable eGaN performance.



Switching regulators: migration path



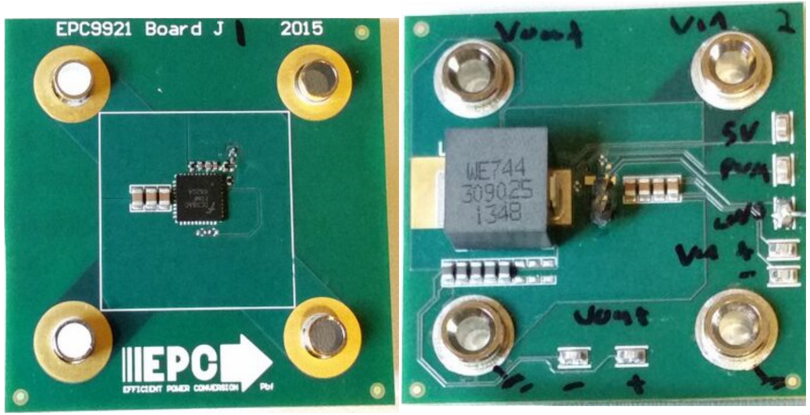
2014-10-18
21:50:32

```
Horizontal
Res: 100 ps / 10 GSa/s
RL:  4 kSa
Scl:  40 ns/div
Pos: 69.5 ns
Trigger                Auto
A:    Edge  Ch1
Lvl:  2.5037 V

Ch1Wfm1
Pos: -2.5 div
Off:  0 V
Scl:  2 V/div
Cpl: DC 50Ω
Dec:Sa | TA: Off

Meas Result 1
RTime    1.3508 ns
FTime    1.3527 ns
```

Higher speed eGaN devices can create significant ringing on the drain voltage generating EMI and increasing voltage stress

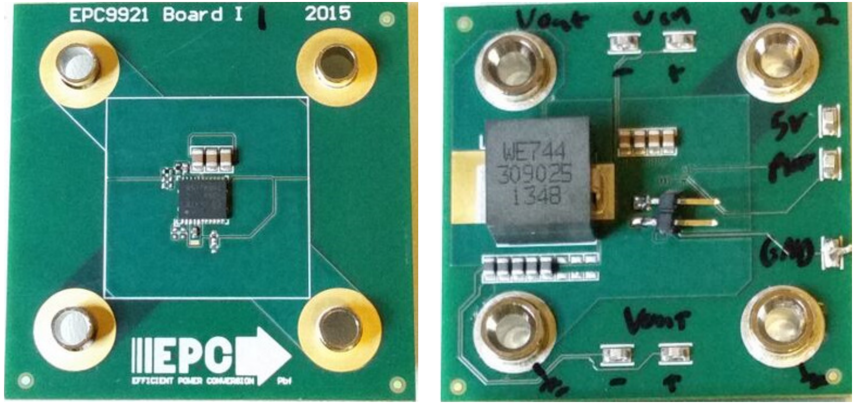
Linear regulators: migration path example

Si FET based



VS.

eGaN based



- **Smaller design:** Space saver

Switching regulators: Efficiency

- **Power conversion efficiency depends on the dynamic power losses that occur during the transition of transistors from on to off and vice-versa.**
  - The total loss is lower in eGaN based switching regulator, provided the conduction loss is controlled.

Regulator Losses	Key Switch Device Parameters	Si MOSFET	eGaN HEMT	Winner
Switching loss	Gate charge	Higher	Lower	eGaN
Reverse conduction loss	Body diode drop	Lower	Higher	Si
Capacitance loss	Device capacitance	Higher	Lower	eGaN
Reverse recovery loss	Reverse recovery charge	Higher	Lower, nearly zero.	eGaN
Gate charge loss	Gate charge	Higher	Lower	eGaN

Switching regulators: switching node waveforms

The eGaN waveform are found to have sharper transitions.

Keysight Infiniium : Friday, August 21, 2015 3:10:43 PM

Measurement	Current	Mean	Min	Max	Range (Max-Min)	Std Dev	Count
V max(1)	11.9868 V	11.9868 V	11.9868 V	11.9868 V	0.0 V	0.0 V	1
Fall time(1)	2.36057 ns	2.36057 ns	2.36057 ns	2.36057 ns	0.0 s	0.0 s	1
Rise time(1)	Edge?	0.0 s	0.0 s	0.0 s	0.0 s	0.0 s	0

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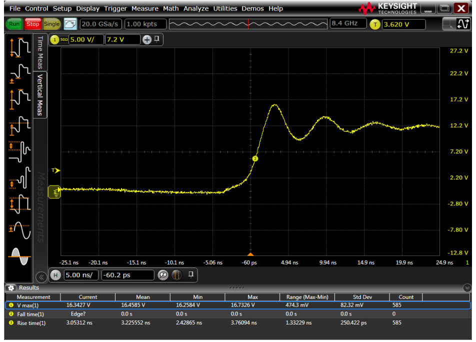

Measurement	Current	Mean	Min	Max	Range (Max-Min)	Std Dev	Count
V max(1)	16.3427 V	16.4585 V	16.2584 V	16.7326 V	474.3 mV	82.32 mV	585
Fall time(1)	Edge?	0.0 s	0.0 s	0.0 s	0.0 s	0.0 s	0
Rise time(1)	3.05312 ns	3.225552 ns	2.42865 ns	3.76094 ns	1.33229 ns	250.422 ps	585

Fairchild DrMOS LTC3891

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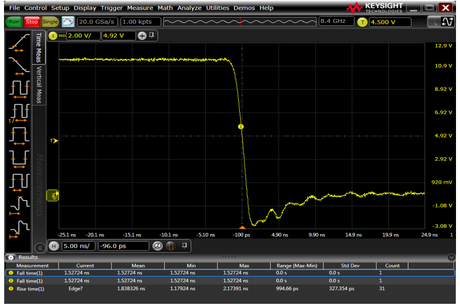

Measurement	Current	Mean	Min	Max	Range (Max-Min)	Std Dev	Count
Fall time(1)	1.52724 ns	1.52724 ns	1.52724 ns	1.52724 ns	0.0 s	0.0 s	1
Fall time(1)	1.52724 ns	1.52724 ns	1.52724 ns	1.52724 ns	0.0 s	0.0 s	1
Rise time(1)	Edge?	1.838326 ns	1.17924 ns	2.17391 ns	994.66 ps	327.354 ps	31

Keysight Infiniium : Friday, August 21, 2015 1:52:03 PM

Measurement	Current	Mean	Min	Max	Range (Max-Min)	Std Dev	Count
V max(1)	14.5907 V	14.5907 V	14.5907 V	14.5907 V	0.0 V	0.0 V	1
Fall time(1)	Edge?	0.0 s	0.0 s	0.0 s	0.0 s	0.0 s	0
Rise time(1)	2.07380 ns	2.07380 ns	2.07380 ns	2.07380 ns	0.0 s	0.0 s	1

eGaN LTC3891

Switching regulators: Gate drive voltage stability

The PCB layout parasitic inductance is minimized in order to keep the gate voltage below 6V.

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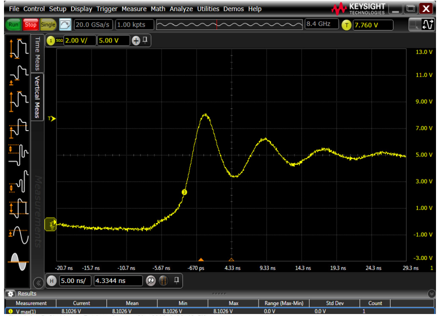


Measurement	Current	Mean	Min	Max	Range (Max-Min)	Std Dev	Count
V max(1)	8.1026 V	8.1026 V	8.1026 V	8.1026 V	0.0 V	0.0 V	1

Keysight Infiniium : Friday, August 21, 2015 3:13:42 PM

Measurement	Current	Mean	Min	Max	Range (Max-Min)	Std Dev	Count
V max(1)	4.9678 V	4.96556 V	4.9320 V	5.0268 V	94.9 mV	14.73 mV	180
Fall time(1)	1.68292 ns	1.701708 ns	1.55789 ns	1.77654 ns	218.65 ps	41.503 ps	180
Rise time(1)	Edge?	0.0 s	0.0 s	0.0 s	0.0 s	0.0 s	0

Fairchild DrMOS LTC3891

Keysight Infiniium : Friday, August 21, 2015 1:59:11 PM

Measurement	Current	Mean	Min	Max	Range (Max-Min)	Std Dev	Count
V max(1)	5.9490 V	5.9490 V	5.9490 V	5.9490 V	0.0 V	0.0 V	1
Fall time(1)	Edge?	0.0 s	0.0 s	0.0 s	0.0 s	0.0 s	0
Rise time(1)	1.73112 ns	1.73112 ns	1.73112 ns	1.73112 ns	0.0 s	0.0 s	1

Keysight Infiniium : Friday, August 21, 2015 1:57:57 PM

Measurement	Current	Mean	Min	Max	Range (Max-Min)	Std Dev	Count
V max(1)	4.8373 V	4.83750 V	4.8225 V	4.8689 V	46.4 mV	8.76 mV	78
Fall time(1)	1.13758 ns	1.134880 ns	1.08923 ns	1.18452 ns	95.30 ps	19.429 ps	78
Rise time(1)	Edge?	0.0 s	0.0 s	0.0 s	0.0 s	0.0 s	0

eGaN LTC3891

Switching regulators: EMI

Emissions are quite different for the eGaN HEMT and Si MOSFET devices, especially at the higher frequency.

Fairchild DrMOS LTC3891


RBW 3.0 MHz
PNO: Fast IFGain:Low
Trig: Free Run
Atten: 10 dB
Avg Type: Log-Pwr
Avg|Hold:>100/100
12:48:04 PM Aug 21, 2015
Mkr1 250.500 MHz -54.174 dBm
10 dB/div Ref 0.00 dBm
Start 1.0 MHz Stop 500.0 MHz
Res BW 3.0 MHz VBW 50 MHz Sweep 1.000 ms (1001 pts)
AC coupled: Accy unspec'd < 10MHz

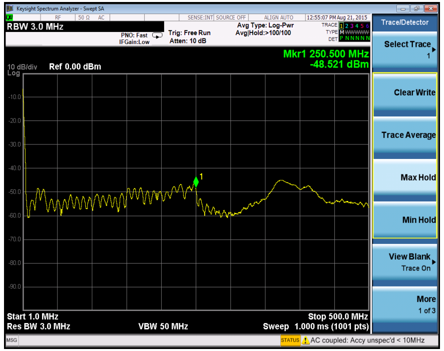
E field at Si MOSFET


RBW 3.0 MHz
PNO: Fast IFGain:Low
Trig: Free Run
Atten: 10 dB
Avg Type: Log-Pwr
Avg|Hold:>100/100
12:46:15 PM Aug 21, 2015
Mkr1 250.500 MHz -32.961 dBm
10 dB/div Ref 0.00 dBm
Start 1.0 MHz Stop 500.0 MHz
Res BW 3.0 MHz VBW 50 MHz Sweep 1.000 ms (1001 pts)
AC coupled: Accy unspec'd < 10MHz

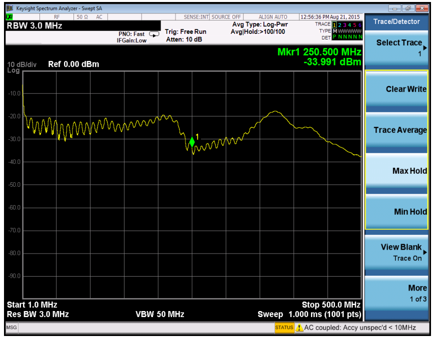
H field at Si MOSFET

VS.

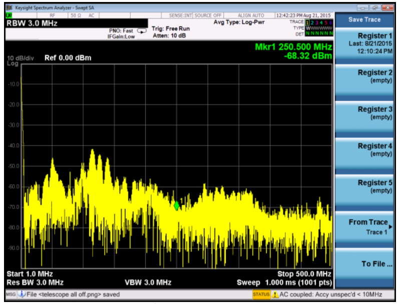
eGaN LTC3891


RBW 3.0 MHz
PNO: Fast IFGain:Low
Trig: Free Run
Atten: 10 dB
Avg Type: Log-Pwr
Avg|Hold:>100/100
12:55:07 PM Aug 21, 2015
Mkr1 250.500 MHz -48.521 dBm
10 dB/div Ref 0.00 dBm
Start 1.0 MHz Stop 500.0 MHz
Res BW 3.0 MHz VBW 50 MHz Sweep 1.000 ms (1001 pts)
AC coupled: Accy unspec'd < 10MHz

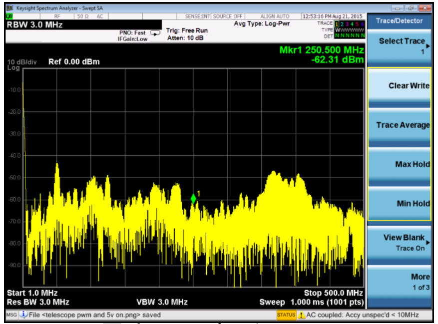
E field at eGaN HEMT


RBW 3.0 MHz
PNO: Fast IFGain:Low
Trig: Free Run
Atten: 10 dB
Avg Type: Log-Pwr
Avg|Hold:>100/100
12:56:36 PM Aug 21, 2015
Mkr1 250.500 MHz -33.991 dBm
10 dB/div Ref 0.00 dBm
Start 1.0 MHz Stop 500.0 MHz
Res BW 3.0 MHz VBW 50 MHz Sweep 1.000 ms (1001 pts)
AC coupled: Accy unspec'd < 10MHz

H field at eGaN HEMT


RBW 3.0 MHz
PNO: Fast IFGain:Low
Trig: Free Run
Atten: 10 dB
Avg Type: Log-Pwr
12:42:23 PM Aug 21, 2015
Mkr1 250.500 MHz -68.32 dBm
10 dB/div Ref 0.00 dBm
Start 1.0 MHz Stop 500.0 MHz
Res BW 3.0 MHz VBW 3.0 MHz Sweep 1.000 ms (1001 pts)
File <telescope all off.png> saved
AC coupled: Accy unspec'd < 10MHz

Telescopic Antenna


RBW 3.0 MHz
PNO: Fast IFGain:Low
Trig: Free Run
Atten: 10 dB
Avg Type: Log-Pwr
12:53:16 PM Aug 21, 2015
Mkr1 250.500 MHz -62.31 dBm
10 dB/div Ref 0.00 dBm
Start 1.0 MHz Stop 500.0 MHz
Res BW 3.0 MHz VBW 3.0 MHz Sweep 1.000 ms (1001 pts)
File <telescope pwm and 5v on.png> saved
AC coupled: Accy unspec'd < 10MHz

Telescopic Antenna

Conclusion

- **Existing linear regulator designs can directly benefit from replacing the Si BJT or MOSFET with eGaN HEMT** :
  - As part of this migration, it is also possible to increase the operating bandwidth of the regulator further improving the performance.

- **For switching regulators, migration from Si MOSFET to eGaN HEMT is complex and we cannot take full advantage of eGaN technology simply by changing the switches from Si to eGaN.**
  - It is generally necessary to design it for eGaN from the start.
  - Optimized eGaN HEMT based switching regulator design will outperform a Si MOSFET based solution in most cases.

Thank you!

QUESTIONS?